SERVICE MANUAL

Model:

PDP-5025M Monitor

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Technical Specifications
Block Diagram
Circuit Diagram
Basic Operations & Circuit Description
Main IC Specifications
Trouble Shooting Manual of PDP Module
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Software Upgrade

This manual is the latest at the time of printing, and does not include the modification which may be made after the printing, by the constant improvement of product.

Safety Precaution

CAUTION

RISK OF ELECTRIC SHOCK
DO NOT OPEN

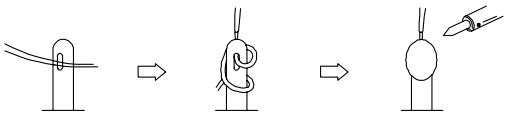
CAUTION: TO REDUCE THE RISK OF ELECTRIC SHOCK, DO NOT REMOVE COVER (OR BACK). NO USER-SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL ONLY.

The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated “dangerous voltage” within the product’s enclo sure that may be of sufficient magnitude to constitute a risk of electric shock to persons.

The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.

PRECAUTIONS DURING SERVICING

1. In addition to safety, other parts and assemblies are specified for conformance with such regulations as those applying to spurious radiation. These must also be replaced only with specified replacements.
   Examples: RF converters, tuner units, antenna selection switches, RF cables, noise-blocking capacitors, noise-blocking filters, etc.
2. Use specified internal Wiring. Note especially:
   1) Wires covered with PVC tubing
   2) Double insulated wires
   3) High voltage leads
3. Use specified insulating materials for hazardous live parts. Note especially:
   1) Insulating Tape
   2) PVC tubing
   3) Spacers (insulating barriers)
   4) Insulating sheets for transistors
   5) Plastic screws for fixing micro switches
4. When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.), wrap ends of wires securely about the terminals before soldering.



5. Make sure that wires do not contact heat generating parts (heat sinks, oxide metal film resistors, fusible resistors, etc.)
6. Check if replaced wires do not contact sharply edged or pointed parts.
7. Make sure that foreign objects (screws, solder droplets, etc.) do not remain inside the set.

MAKE YOUR CONTRIBUTION TO PROTECT THE ENVIRONMENT

Used batteries with the ISO symbol for recycling as well as small accumulators (rechargeable batteries), mini-batteries (cells) and starter batteries should not be thrown into the garbage can.

Please leave them at an appropriate depot.

WARNING:

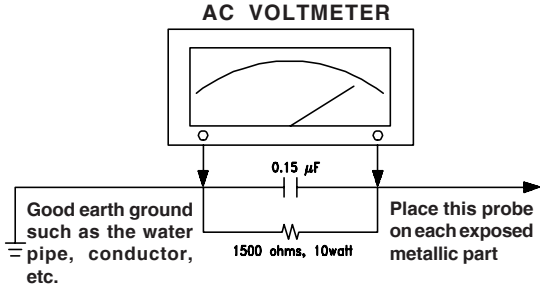
Before servicing this TV receiver, read the SAFETY INSTRUCTION and PRODUCT SAFETY NOTICE.

SAFETY INSTRUCTION

The service should not be attempted by anyone unfamiliar with the necessary instructions on this apparatus. The following are the necessary instructions to be observed before servicing.

1. An isolation transformer should be connected in the power line between the receiver and the AC line when a service is performed on the primary of the converter transformer of the set.
2. Comply with all caution and safety related provided on the back of the cabinet, inside the cabinet, on the chassis or picture tube.
3. To avoid a shock hazard, always discharge the picture tube's anode to the chassis ground before removing the anode cap.
4. Completely discharge the high potential voltage of the picture tube before handling. The picture tube is a vacuum and if broken, the glass will explode.

5. When replacing a MAIN PCB in the cabinet, always be certain that all protective are installed properly such as control knobs, adjustment covers or shields, barriers, isolation resistor networks etc.
6. When servicing is required, observe the original lead dressing. Extra precaution should be given to assure correct lead dressing in the high voltage area.
7. Keep wires away from high voltage or high tempera ture components.
8. Before returning the set to the customer, always perform an AC leakage current check on the exposed metallic parts of the cabinet, such as antennas, terminals, screwheads,metal overlay, control shafts, etc., to be sure the set is safe to operate without danger of electrical shock. Plug the AC line cord directly to the AC outlet (do not use a line isolation transformer during this check). Use an AC voltmeter having 5K ohms volt sensitivity or more in the following manner.
   Connect a 1.5K ohm 10 watt resistor paralleled by a 0.15μF AC type capacitor, between a good earth ground (water pipe, conductor etc.,) and the exposed metallic parts, one at a time. Measure the AC voltage across the combination of the 1.5K ohm resistor and 0.15 uF capacitor. Reverse the AC plug at the AC outlet and repeat the AC voltage measurements for each exposed metallic part.
   The measured voltage must not exceed 0.3V RMS.
   This corresponds to 0.5mA AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.
   The resistance measurement should be done between accessible exposed metal parts and power cord plug prongs with the power switch "ON". The resistance should be more than 6M ohms.



AC Leakage Current Check

PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in this apparatus have special safety-related characteristics.

These characteristics are offer passed unnoticed by visual spection and the protection afforded by them cannot necessarily be obtained by using replacement components rates for a higher voltage, wattage, etc.

The replacement parts which have these special safety characteristics are identified by ⚠ marks on the schematic diagram and on the parts list.

Before replacing any of these components, read the parts list in this manual carefully. The use of substitute replacement parts which do not have the same safety characteristics as specified in the parts list may create shock, fire, or other hazards.

9. Must be sure that the ground wire of the AC inlet is connected with the ground of the apparatus properly.

Technical Specifications	MODEL : ***PDP-5025M Monitor*** 50" Plasma Display			
DATE FIRST ISSUED	ISSUE 1	RAISED BY	CHECKED BY	NUMBER OF PAGE 10

RAISED BY :

DATE		
R & D DEPARTMENT	.....	.....
COMMERCIAL DEPARTMENT	.....	.....
PRODUCTION DEPARTMENT	.....	.....
Q/A DEPARTMENT	.....	.....
CUSTOMER	.....	.....
	.....	.....

SIGNATURE : DATE :

NOTE : Only documents stamped "Controlled Document" to be used for manufacture of production parts.

1. Standard Test Conditions

All tests shall be performed under the following conditions, unless otherwise specified.

1.1 Ambient light : 150ux (When measuring I_B, the ambient luminance $\leqq 0.1Cd/m^2$)

1.2 Viewing distance : 50cm in front of PDP

1.3 Warm up time : 30 minutes

1.4 PDP Panel facing : no restricted

1.5 Measuring Equipment : PC, Chroma 2225 signal generator (with Chroma digital additional card) or equivalent, Minolta CA100 photometer

1.6 Magnetic field : no restricted

1.7 Control settings : Brightness, Contrast, Tint, Color set at Center(50)

1.8 Power input : 100~120Vac

1.9 Ambient temperature : 20°C ± 5°C (68°F ± 9°F)

1.10 Display mode : 31.5KHz/60Hz (Resolution 1366 x 768)

1.11 Other conditions :

1.11.1 With image sticking protection of PDP module, the luminance will descend by time on a same still screen and rapidly go down in 5 minutes. When measuring the color tracking and luminance of a same still screen, be sure t o accomplish the measurement in one minute to ensure its accuracy.

1.11.2 Due to the structure of PDP, the extra-high-bright same screen should not hold over 5 minutes for fear of branding on the panel.

ELECTRICAL CHARACTERISTICS

2. Power Input

2.1	Voltage	:	100 ~120VAC
2.2	Input Current	:	5.0 /2.5A
2.3	Maximum Inrush Current	:	<30 A (FOR AC110V ONLY)
	Test condition	:	Measured when switched off for at least 20 mins
2.4	Frequency	:	50Hz to 60Hz(±3Hz)
2.5	Power Consumption	:	450W Typical
	Test condition	:	full white display with maximum brightness and contrast
2.6	Power Factor	:	Meets IEC1000-3-2
2.7	Withstanding voltage	:	1.5kVac or 2.2kVdc for 1 sec

3. Display

3.1	Screen Size	:	50” Plasma display
3.2	Aspect Ratio	:	16:9
3.3	Pixel Resolution	:	1366x768
3.4	Peak Brightness	:	1000 cd/m² (Typical, Panel only)
3.5	Contrast Ratio (Dark room)	:	5000:1 (Ratio, Typical, in a dark room, Panel only)
3.6	Viewing Angle	:	Over 160°
3.7	OSD language	:	English,Spanish,French

4. Signal

4.1 AV & Graphic input

4.1.1 Composite signal	:	CVBS
4.1.2 Y,C Signal	:	S-Video
4.1.3 Component signal	:	Y PbPr1, YPbPr2, HDMI compatible
4.1.4 Graphic I/P	:	Analog: D-sub 15pin detachable cable Digital : HDMII
4.1.5EDID compatibility	:	DDC 1.3
4.1.6 I/P frequency	:	f_H: 31.5kHz to 60kHz/f_V: 56.25Hz to 75Hz (1024X768 recommended)

4.2 Audio input VGA (D-Sub 15 pin Type) ×1
D-Sub 9 Pin (RS-232 Input) × 1
HDMI (Ver. 1.1) connector × 1
S-Video (Mini Din 4 Pin) × 1
Video (RCA Type) × 1
YpbPr1/YpbPr2 × 1
Stereo/Audio × 6

4.3 Audio output Audio (L+R) × 1 Video (RCA Type) × 1 SPDIF (Optical) × 1

PIP/POP/PBP, Picture size, Picture Still, Sound mode,Last memory, Timer, MTS

5. Environment

5.1 Operating environment

5.1.1 Temperature : 5º to 33°C
5.1.2 Relative humidity: 20% to 85%(non-condensing)

5.2 Storage and Transport

5.2.1 Temperature : -20°C to 60°C(-4º to 140°F)
5.2.2 Relative humidity: 5% to 95%

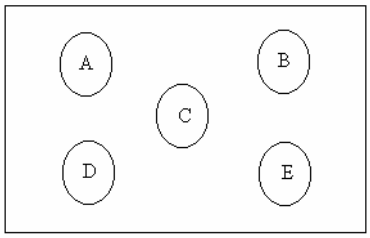
6. Panel Characteristics

6.1 Type : S50HW-XD03
6.2 Size : 50",1106.5mm(W)X622.1mm(H)

6.3 Aspect ratio : 16:9
6.4 Viewing angle : Over 160°
6.5 Resolution : 1366X768
6.6 Weight : 22.0kg ±0.5 kg (Net)
6.7 Color : 16.7 millions of colors (R/G/B each 256 scales)
6.8 Contrast : Average 60:1 (In a bright room with 150Lux at center)
Typical 5000:1 (In a dark room 1/100 White Window pattern at center).
6.9 Peak brightness : Typical 1000cd/㎡ (1/25 White Window)

6.10 Color Coordinate Uniformity : Contrast; Brightness and Color control at normal setting

Test Pattern : Full white pattern



Average of point A,B,C,D and E +/- 0.01

6.11 Color temperature : Contrast at center (50); Brightness center (50);
Color temperature set at Natural
x=0.285±0.02
y=0.290±0.02

6.12 Cell Defect Specifications
Subject to Panel supplier specification as appends.

7. Front Panel Control Button

7.1 SET Up / Down Button : Push the key to select Item up or down.
When selecting the item on OSD menu.

Volume Left/Right Butt : Push the key to increase the volume left or right.
When selecting the adjusting item on OSD menu increase or decrease the data-bar.

Menu Button : Enter to the OSD menu.

Source Select Button : Press this button and use up/down button to sellect the signal sources. AV, S-Video, YPbPr1,YPbPr2 VGA or HDMI.

7.2 Stand by Button : Switch on main power, or switch off to enter power Saving modes.

7.3 Main Power Switch : Turn on or off the unit.

8. OSD Function

8.1 Picture : State (Normal,Dark,Bright,User); Display (Bright,contrast,Color,Hue)
Temp (warm,Cool,Normal,User);
Position (H-posit,V-posit,Phase,H-size,Auto Adjust)

8.2 Sound : Setup (Mode,AVC,Volume,Balance);
Equalizer (120HZ,500HZ,1.5KHZ,5KHZ,10KHZ)
BBE Setup (Gain,Treble,Bass)

8.3 OSD : Size (Panorama,16:9,Normal,Anamorphic,Letter Box,TV Mode)
OSD Set (Language,OSD Position,Time Out)
Option (Burn Protect, Version)
V-Chip , C/C

8.4 Layout : Layout (Full Screen,PIP,Split Screen,Grid,POP 3,POP 12)
PIP Set (Sub Win Source,Sub Win Size,PIP Size.PIP Position)

8.5 Time : Sleep (30Min,60Min,90Min,120Min,180Min)
Wake Up (Time Edit,Volume,TV Mode,Channel)
Time Set

9. Agency Approvals

Safety	UL/FCC/cUL
Emissions	FCC class B

10. Reliability

11.1 MTBF : 20,000 hours(Use moving picture signal at 25°C ambient)

11. Accessories : User manual x1, Remote control x1, Stand x1,
Battery x 2, Accessories box x 1, AC Cable x1

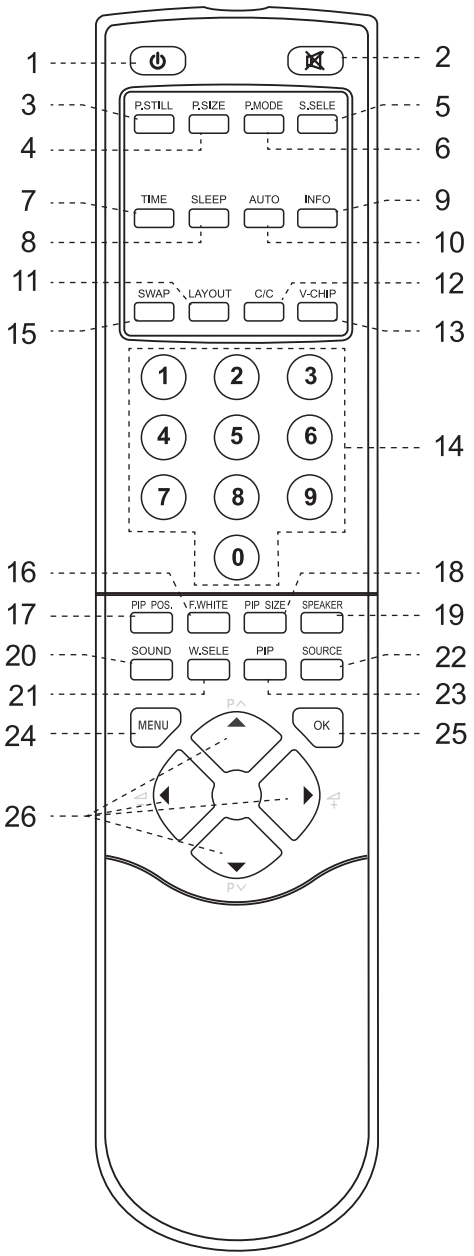
12. Support the Signal Mode

A. HDMI Mode / D-Sub Mode (VGA or DVI) / HDTV Mode (YpbPr1 or YpbPr2)

No	Mode		Resolution	Horizontal Frequency (KHz)	Vertical Frequency (KHz)	Dot Clock Frequency (MHz)
1	HDMI Mode	D-Sub Mode (VGA or DVI)	640x400	31.47	70.08	25.17
2			640x480	31.50	60.00	25.18
3			640x480	35.00	67.00	30.24
4			640x480	37.50	75.00	31.50
5			640x480	37.86	72.81	31.50
6			720x400	31.47	70.08	28.32
7			800x600	31.56	56.25	36.00
8			800x600	37.90	60.32	40.00
9			800x600	46.90	75.00	49.50
10			800x600	48.08	72.19	50.00
11			832x624	49.00	74.00	57.27
12			1024x768	48.84	60.00	65.00
13			1024x768	56.50	70.00	75.00
14			1024x768	60.00	75.00	78.75
15			1152x864	54.53	61.13	80.37
16			1152x864	63.86	70.02	94.51
17			1152x864	67.52	75.02	108.03
18			1280x960	60.02	60.02	108.04
19			1280x1024	64.00	60.01	108.00
20		HDTV Mode (YpbPr1/ YpbPr2)	1080i (1920x1080)	33.75	60.00	74.25
21			1080i (1920x1080)	28.125	50.00	74.25
22			720P (1280x720)	45.00	60.00	74.25
23			720P (1280x720)	37.50	50.00	74.25
24			576p (720x576)	31.25	50.00	27.00
25			480p (720x480)	31.468	59.94	27.00
26			576i	15.625	50.00	13.50
27			480i	15.734	59.94	13.50

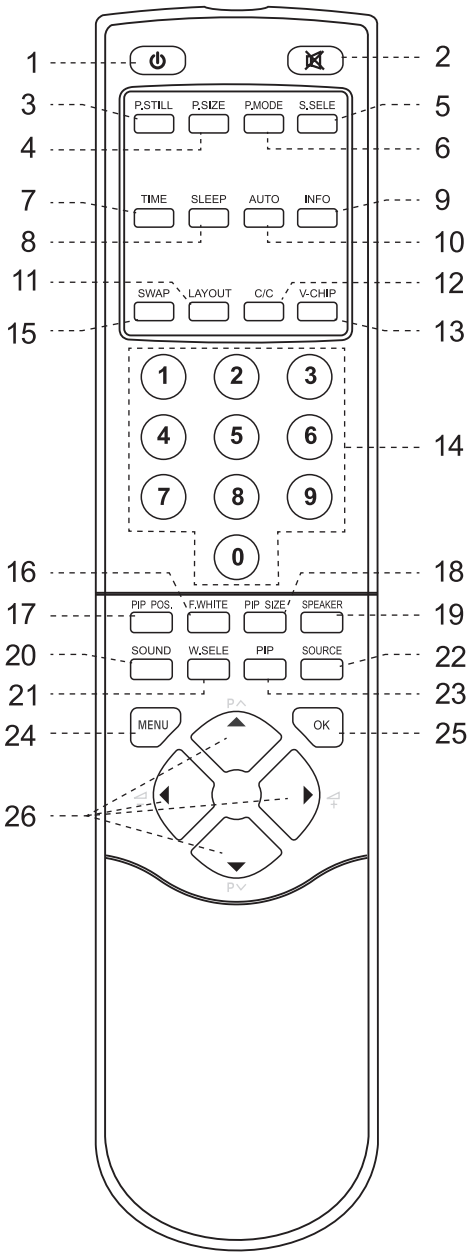
4.4 Remote Control

1 **POWER(⏻):** Press this button to turn off to standby and turn on from standby.
2 **MUTE(🔇):** Press this button to quiet the sound system. Press again to reactivate the sound system.
3 **P.STILL:** Press this button to hold on the screen. Press again to normal.
4 **P.SIZE:** When the input source is YPbPr 1, YPbPr 2, VGA or HDMI, press this button, the picture will change according to Fill All, Force 4:3, Letter Box, Wide or Anamorphic. When the input source is AV or S-Video, press this button, the picture will change according to Fill All, 4:3, Letter Box, Wide or Anamorphic.
5 **S.SELE:** Press this button to select the sound output from Main Window or Sub Window.
6 **P.MODE :** Press the button to select different picture effect.
7 **TIME:** Press this button to pop up the “Clock Set” menu.
8 **SLEEP:** Press this button to select the sleep time.
9 **INFO:** Press the button to display the source information.
10 **AUTO:** The Display automatically adjusts the phase, vertical / horizontal position when pressing this button in VGA mode.
11 **LAYOUT:** Press this button to pop up Layout menu.
12 **C/C:** Press this button to enter the Closed Caption Function. (Only for AV or S-Video)
13 **V-CHIP:** Press this button to enter the V-Chip Function. (Only for AV or S-Video)
14 **Number buttons:** Use these buttons to enter the password.



(Continued on next page)

15 **SWAP:** Press this button to switch the Main window or Sub window pictures in PIP and Split Screen.
16 **F.WHITE:** Press this button to show a full white picture.
17 **PIP POS. :** Press the button to select different Image Position in PIP Mode.
18 **PIP SIZE :** Press the button to select different Image Size in PIP Mode.
19 **SPEAKER:** Press this button to pop up the "Speaker" menu, use the ◀ / ▶ button to select "Internal" or "External".
20 **SOUND:** Press the button to select different sound effect.
21 **W.SELE:** Press this button to select the Main Window or Sub Window.
22 **SOURCE:** Press this button and use ▲ / ▼ button to select the signal sources. AV, S-Video, YPbPr 1, YPbPr 2, VGA or HDMI.
23 **PIP**: Press this button to change different Picture Mode.
24 **MENU:** Press this button to pop up the OSD Menu and press it again to exit the OSD Menu.
25 **OK :** Press to enter or confirm.
26 **◀ / ▶ :** They are used as ◀ / ▶ buttons in the OSD Menu screen and they can be used for the adjustment of volume when the OSD Menu is not shown on the screen.
▲ / ▼ : They are used as ▲ / ▼ buttons in the OSD Menu screen.
They also can be used for the selection of the program when the OSD Menu is not shown on the screen, but only for the Model with Tuner.



PHYSICAL CHARACTERISTICS

14. Power Cord

Length : 1.8m nominal

Type : optional

15. Cabinet

15.1 Color : black colour as defined by colour plaque reference number

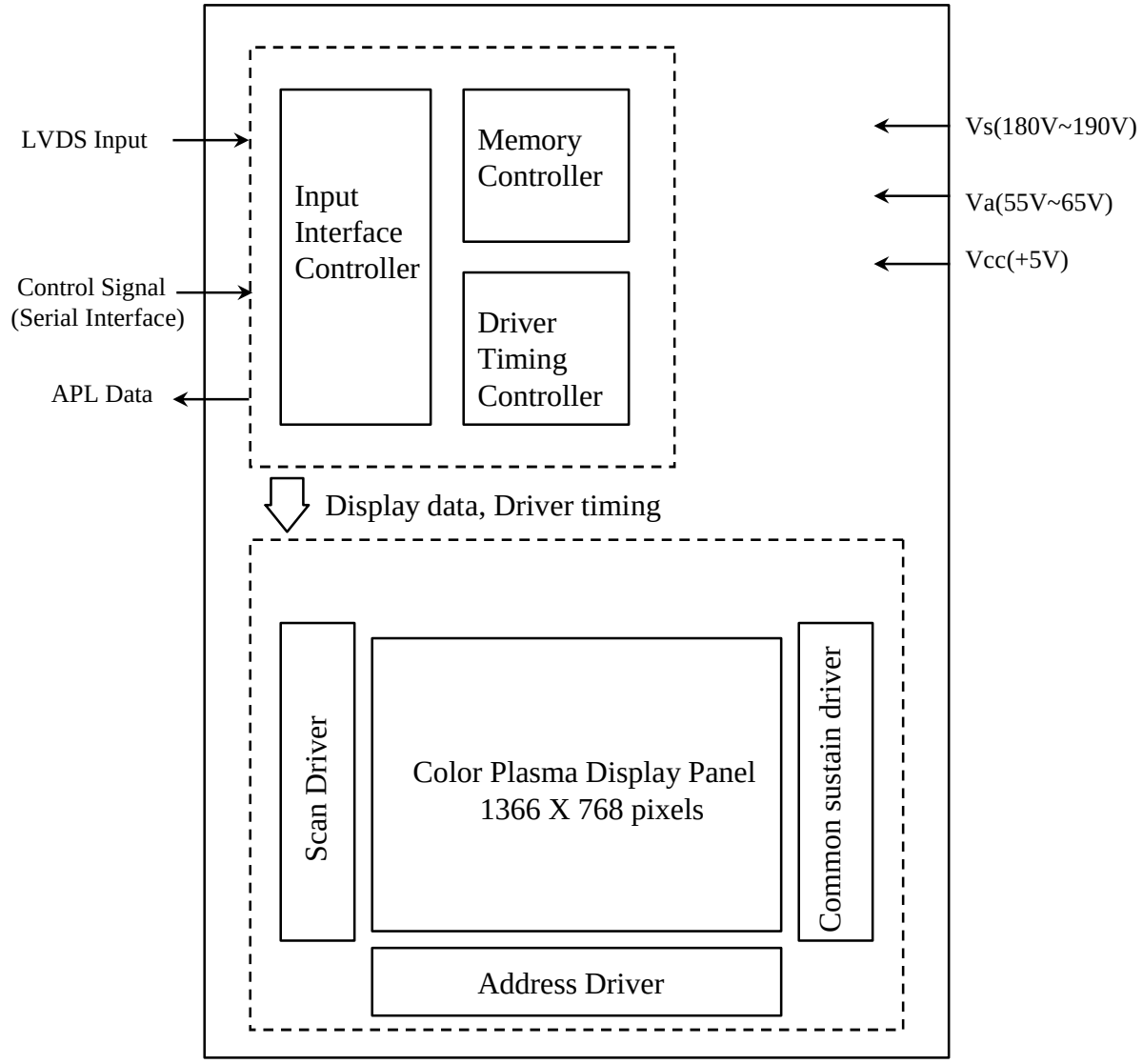
15.2 Weight

Net weight : 51kg
Gross weight : 74kg

15.3 Dimensions (W/O stand&handles)

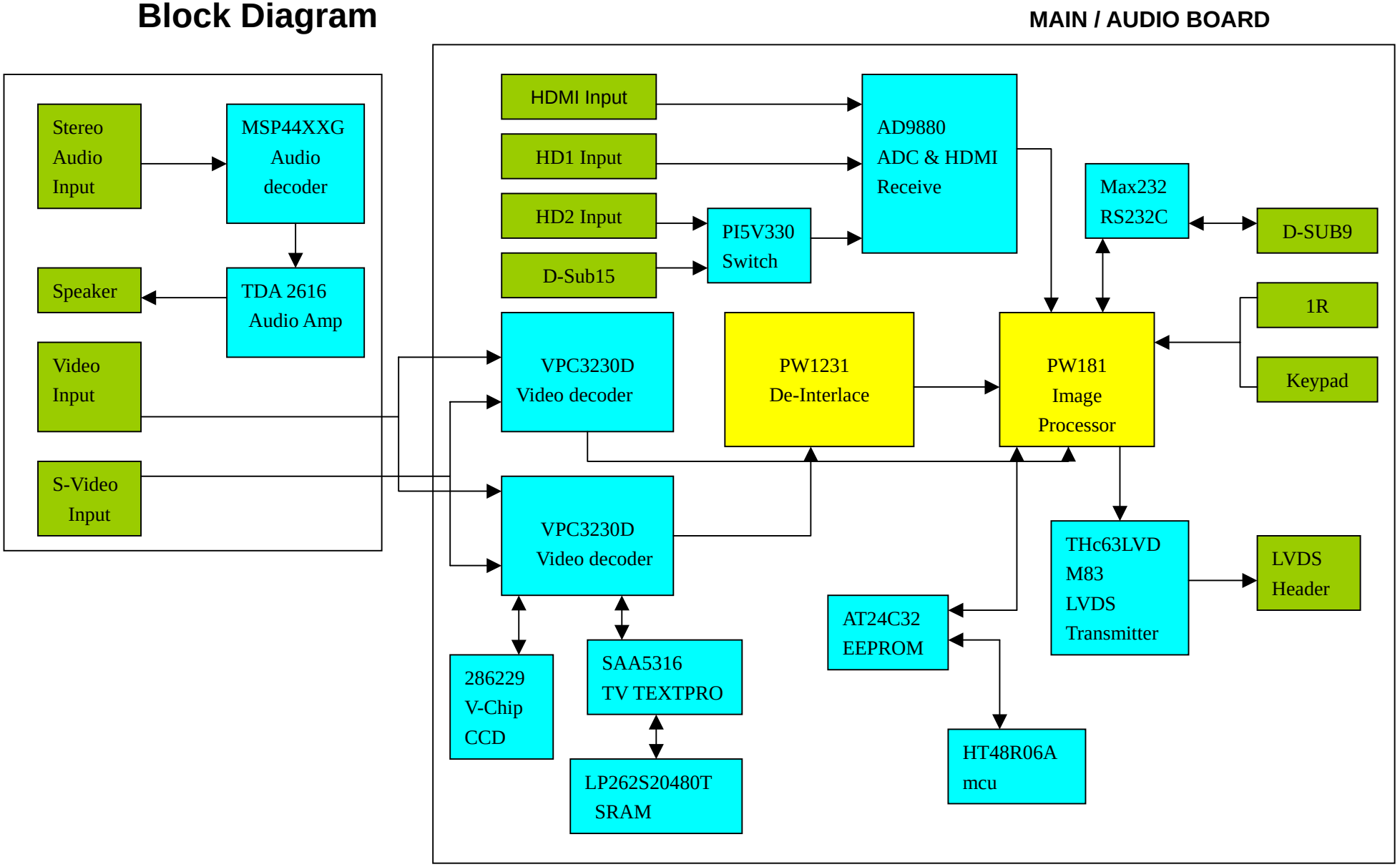
Width : 1227.8mm
Height : 739.8mm
Depth : 100.5mm

Block Diagram



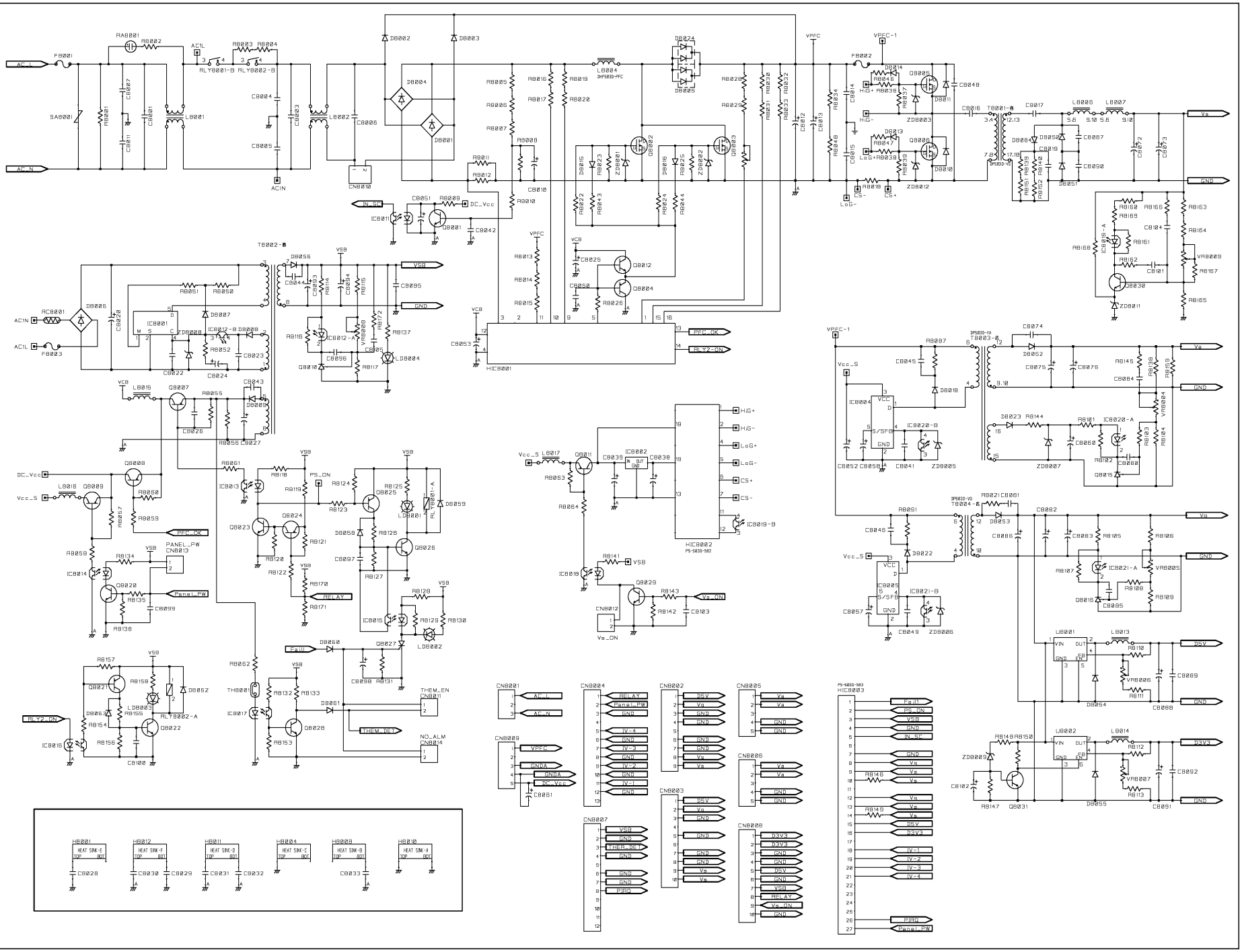
☞ Applied Voltage level is specified at the time when Full-White pattern is displayed on the panel.

Block Diagram



Circuit Diagram

- Power supply board of Audio Amplifier, MPT012A
- Main (Video) board
- Audio/Tuner board
- Keypad board
- Remote control receiver board
- Remote control board


AC_L
AC_N
AC1L
ACIN
FB001
SA8001
RA8001
RA8002
RB001
CB007
CB001
CB011
LB001
RB003
RB004
RLY8001-B
RLY8002-B
CB004
CB003
LB002
CB006
CB005
CN8010
DB002
DB003
DB004
DB001
RB025
RB026
RB027
RB028
RB016
RB017
RB018
RB019
RB020
LB004
DB024
DB025
RB029
RB030
RB031
RB032
RB033
CB012
CB013
VPFC
VPFC-1
FB002
DB014
RB046
HIG+
RB036
Q8005
RB037
HIG-
ZD8003
DB011
CB048
CB016
CB014
RB034
RB040
CB015
LOG+
RB038
DB013
RB047
Q8006
RB039
LOG-
RB018
CS-
CS+
ZD8012
DB010
T8001-B
CB017
LB005
LB007
DB012
DB004
CB025
CB050
RB026
DB015
RB023
ZD8001
DB002
DB016
RB025
ZD8002
DB003
RB022
RB043
RB024
RB044
RB011
RB012
RB010
RB009
DC_Vcc
IN_SC
IC8011
CB051
Q8001
CB042
VCB
VSB
GND
T8002-B
DB056
CB044
CB093
RB114
CB054
RB115
CB095
RB051
RB052
IC8001
DB007
DB008
CB022
CB024
RB052
CB023
AC8001
DB005
CB028
FB003
RB116
IC8012-A
VR8000
RB172
RB137
CB096
RB117
LD8004
Q8010
L8015
Q8007
RB055
CB043
DB009
CB026
RB056
CB027
HIC8001
PFC_OK
RLY2-ON
CB053
RB013
RB014
RB015
CB052
CB045
CB046
CB047
CB048
CB049
CB050
CB051
CB053
CB054
CB055
CB056
CB057
CB058
CB059
CB060
CB061
CB062
CB063
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CB066
CB067
CB068
CB069
CB070
CB071
CB072
CB073
CB074
CB075
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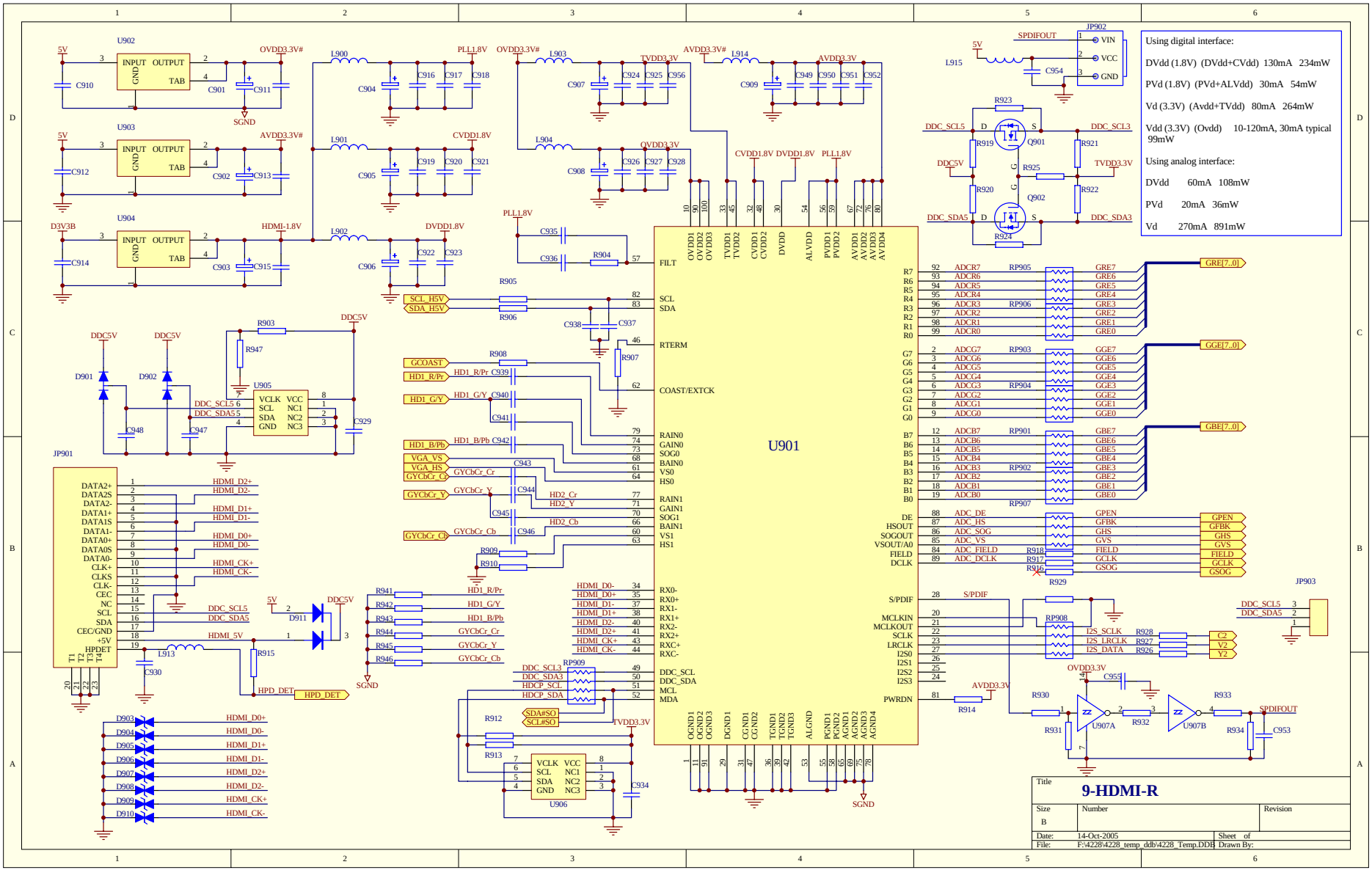
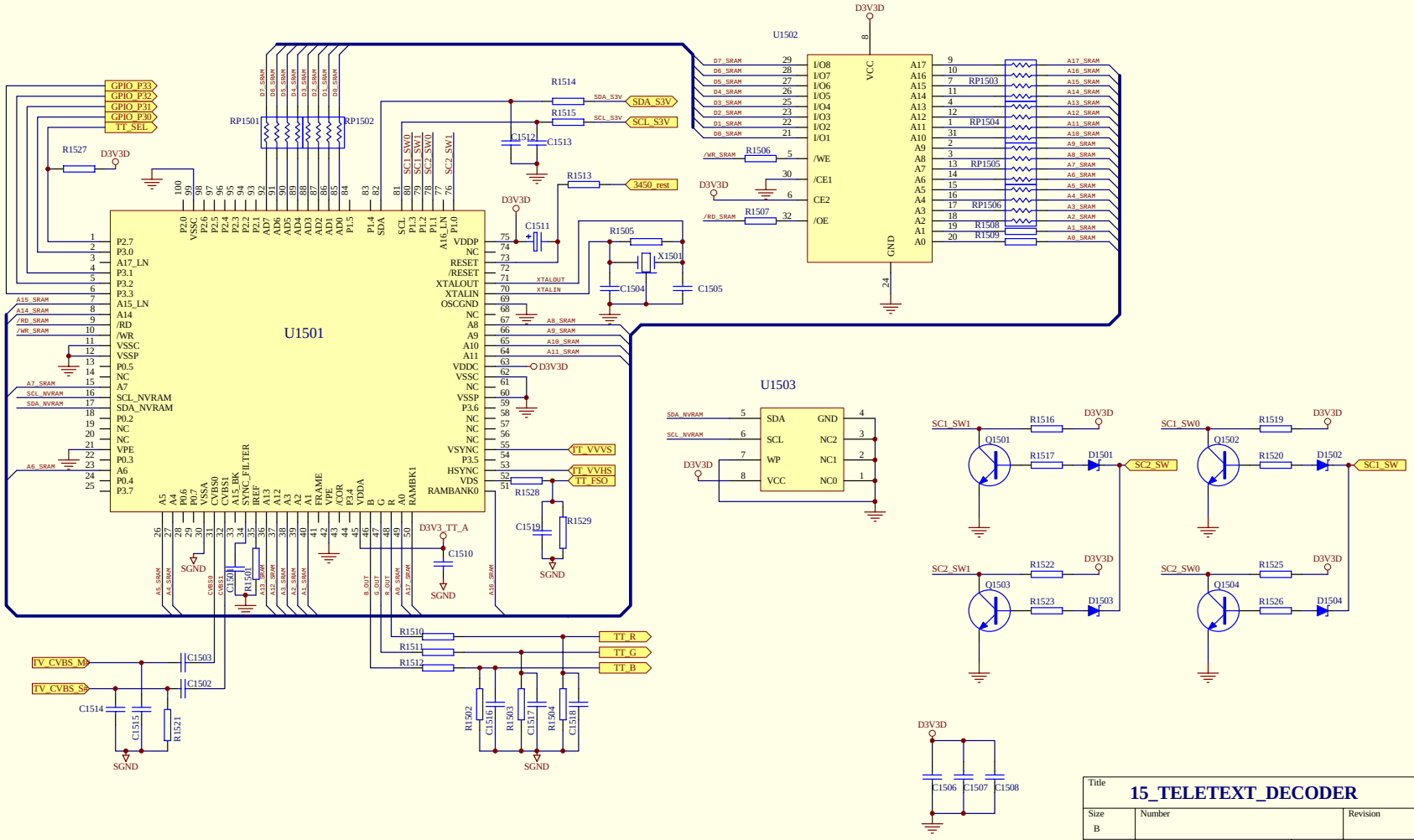
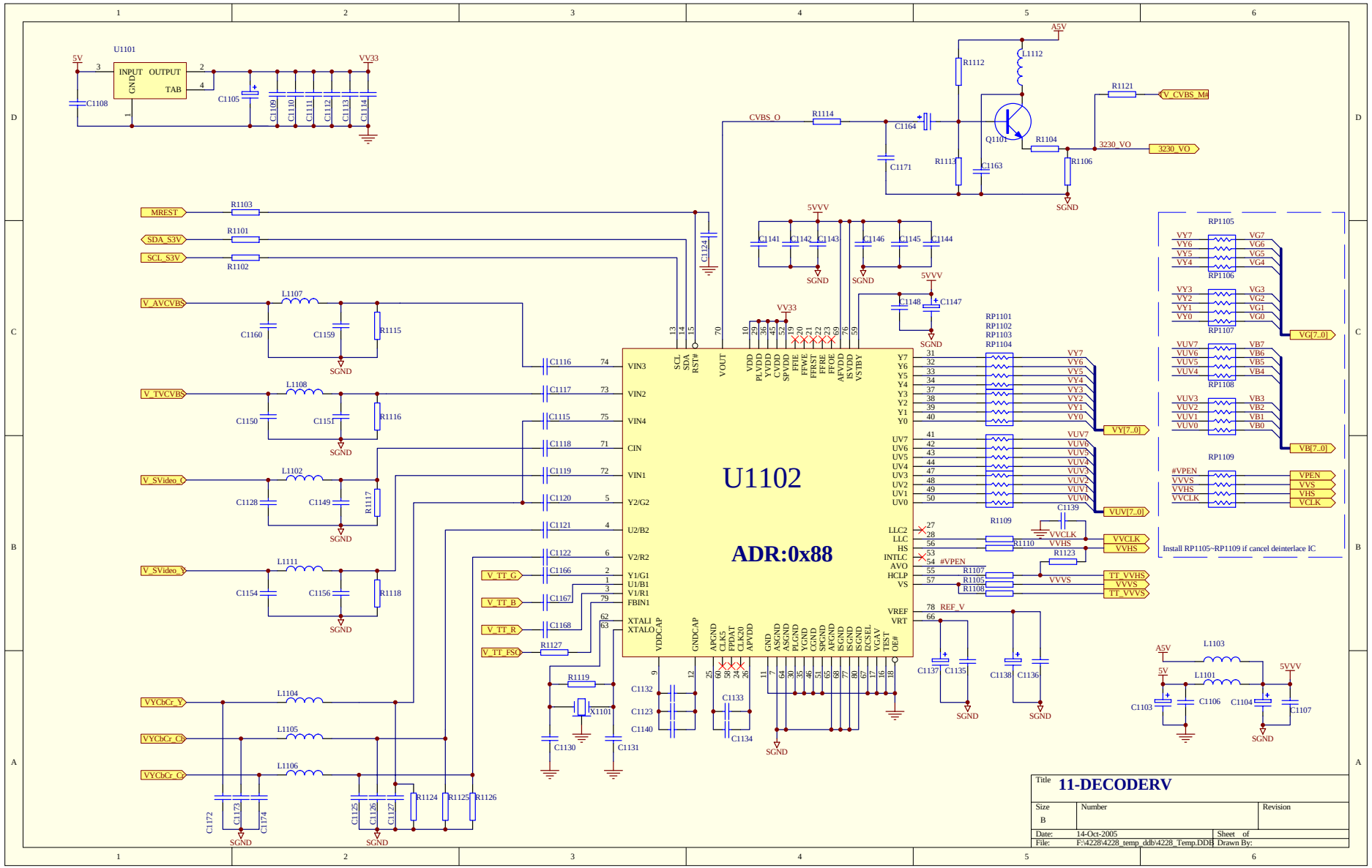
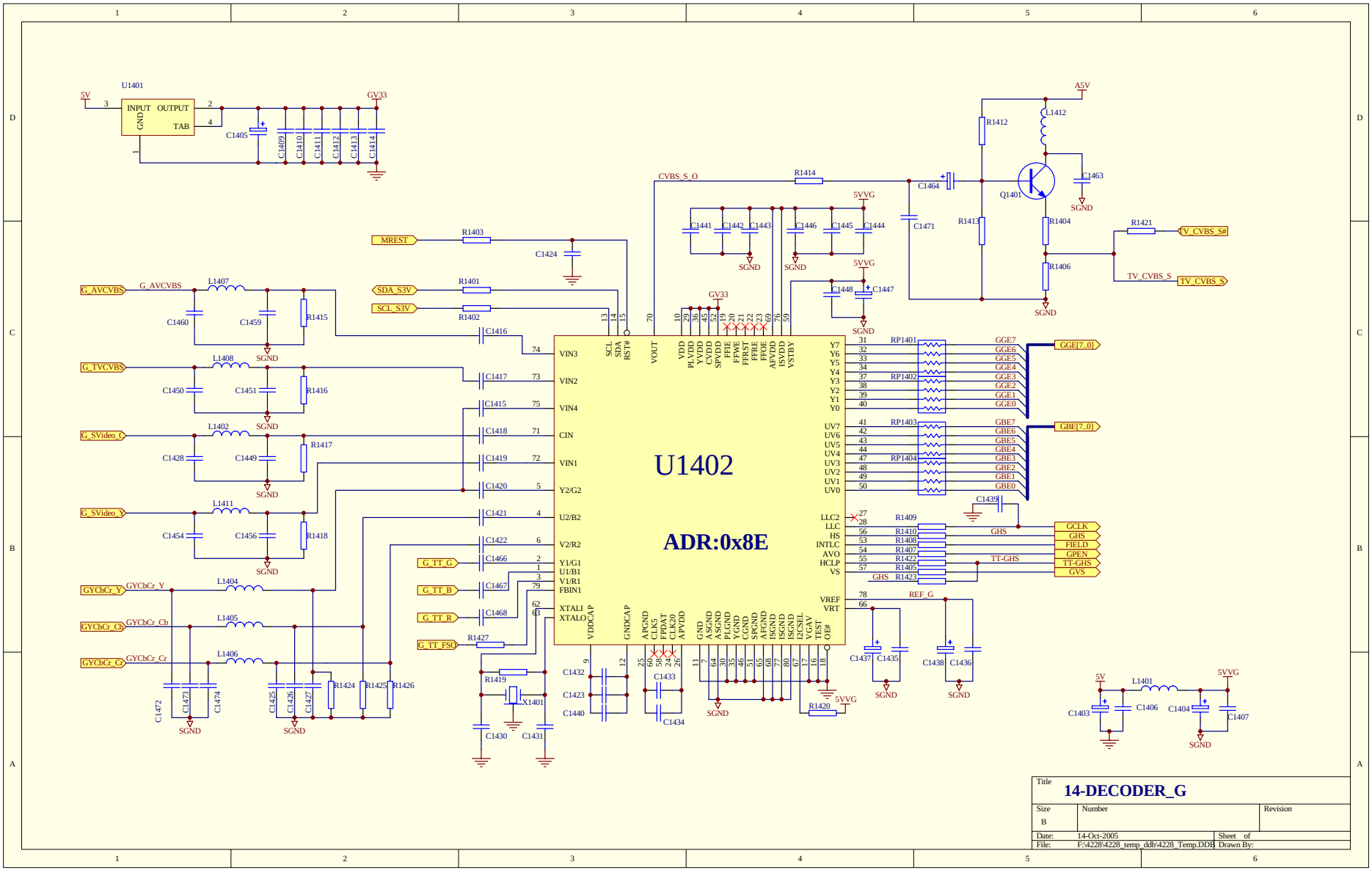
CB078
CB079
CB080
CB081
CB082
CB083
CB084
CB085
CB086
CB087
CB088
CB089
CB090
CB091
CB092

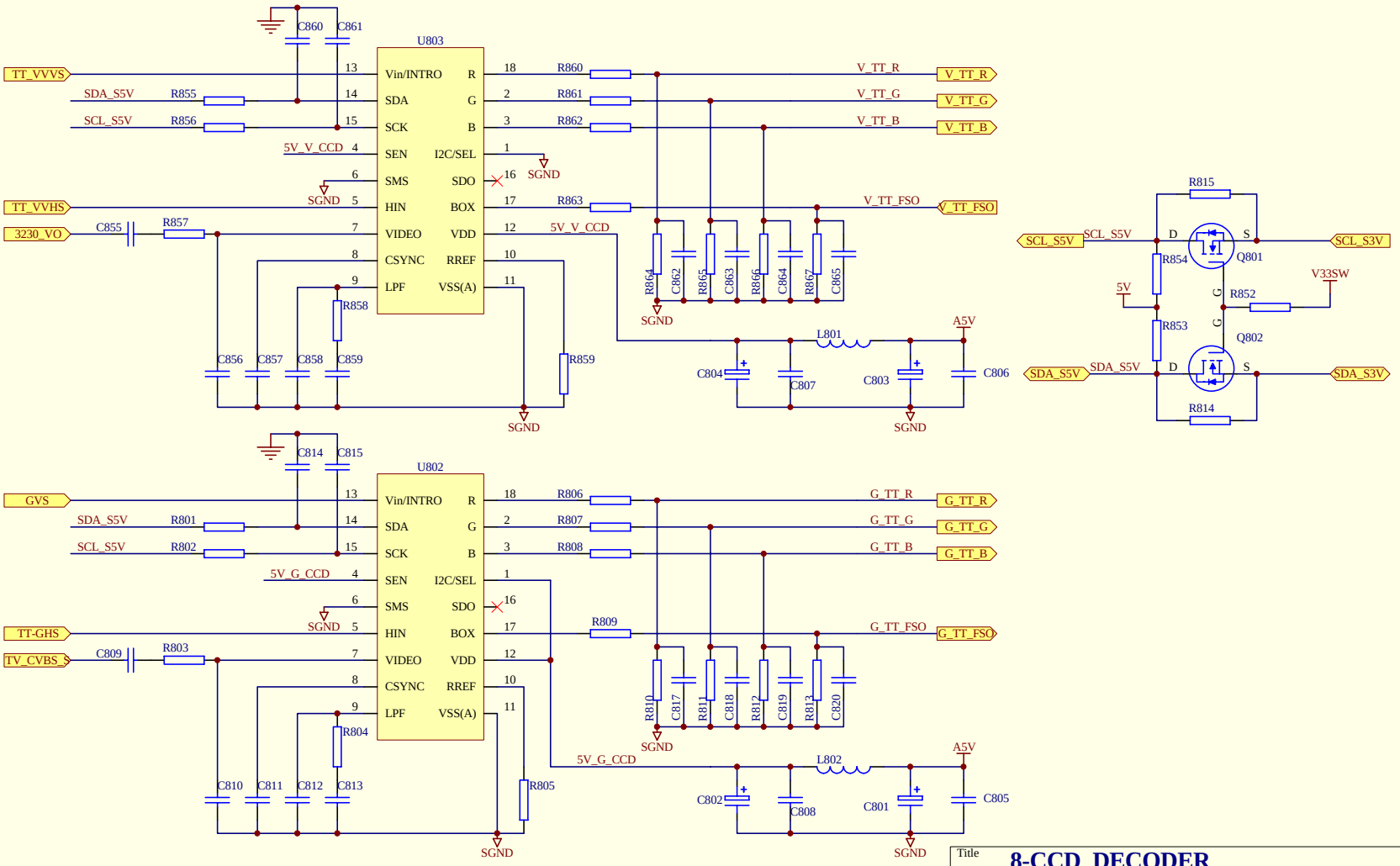

U901
U902
U903
U904
U905
U906
JP901
JP902
JP903
Using digital interface:
DVdd (1.8V) (DVdd+CVdd) 130mA 234mW
PVd (1.8V) (PVd+ALVdd) 30mA 54mW
Vd (3.3V) (Avdd+TVdd) 80mA 264mW
Vdd (3.3V) (Ovdd) 10-120mA, 30mA typical 99mW
Using analog interface:
DVdd 60mA 108mW
PVd 20mA 36mW
Vd 270mA 891mW
Title
9-HDMI-R
Size B
Number
Revision
Date: 14-Oct-2005
Sheet of
File: F:\4228\4228_temp_ddb\4228_Temp.DDB
Drawn By:

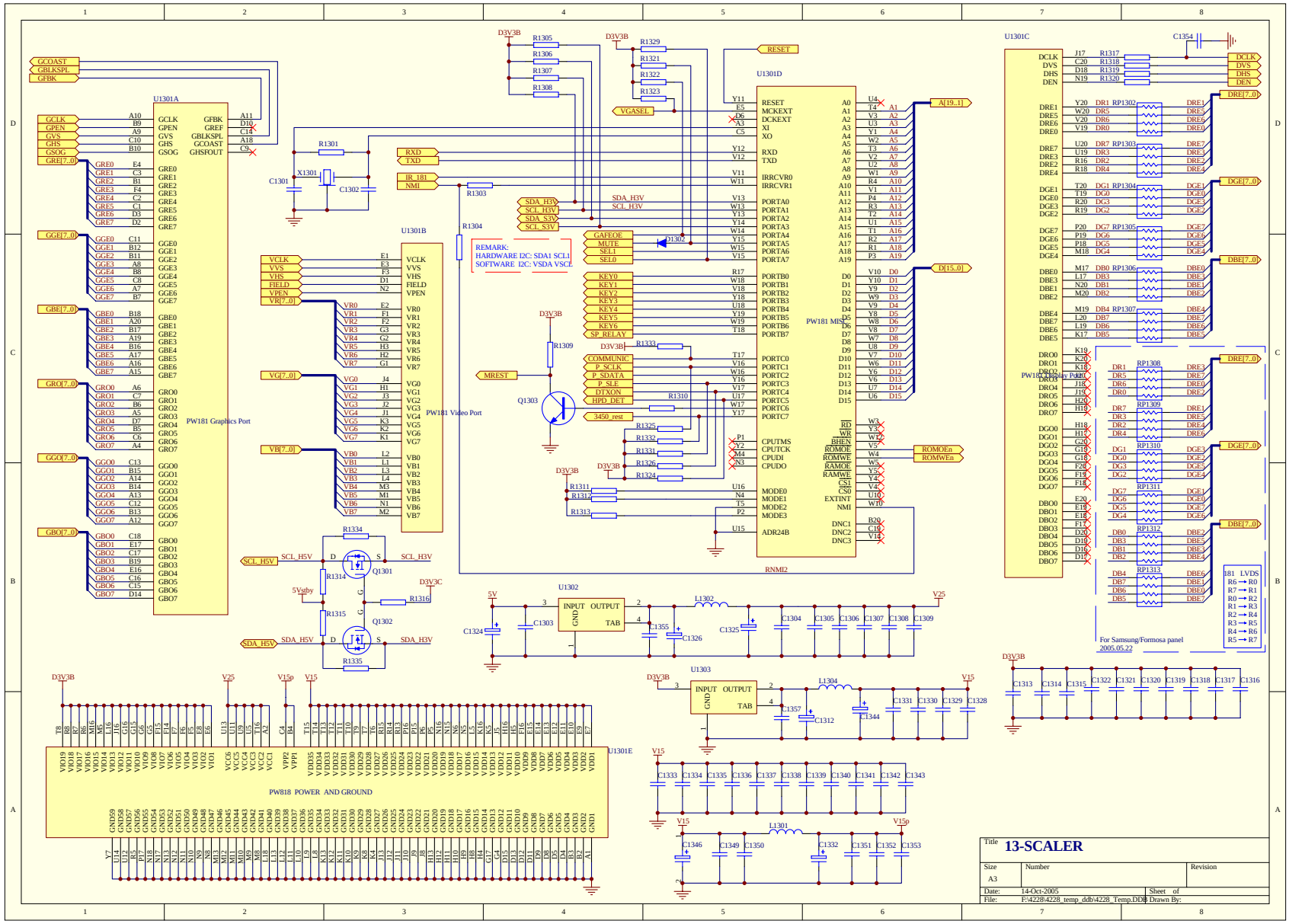


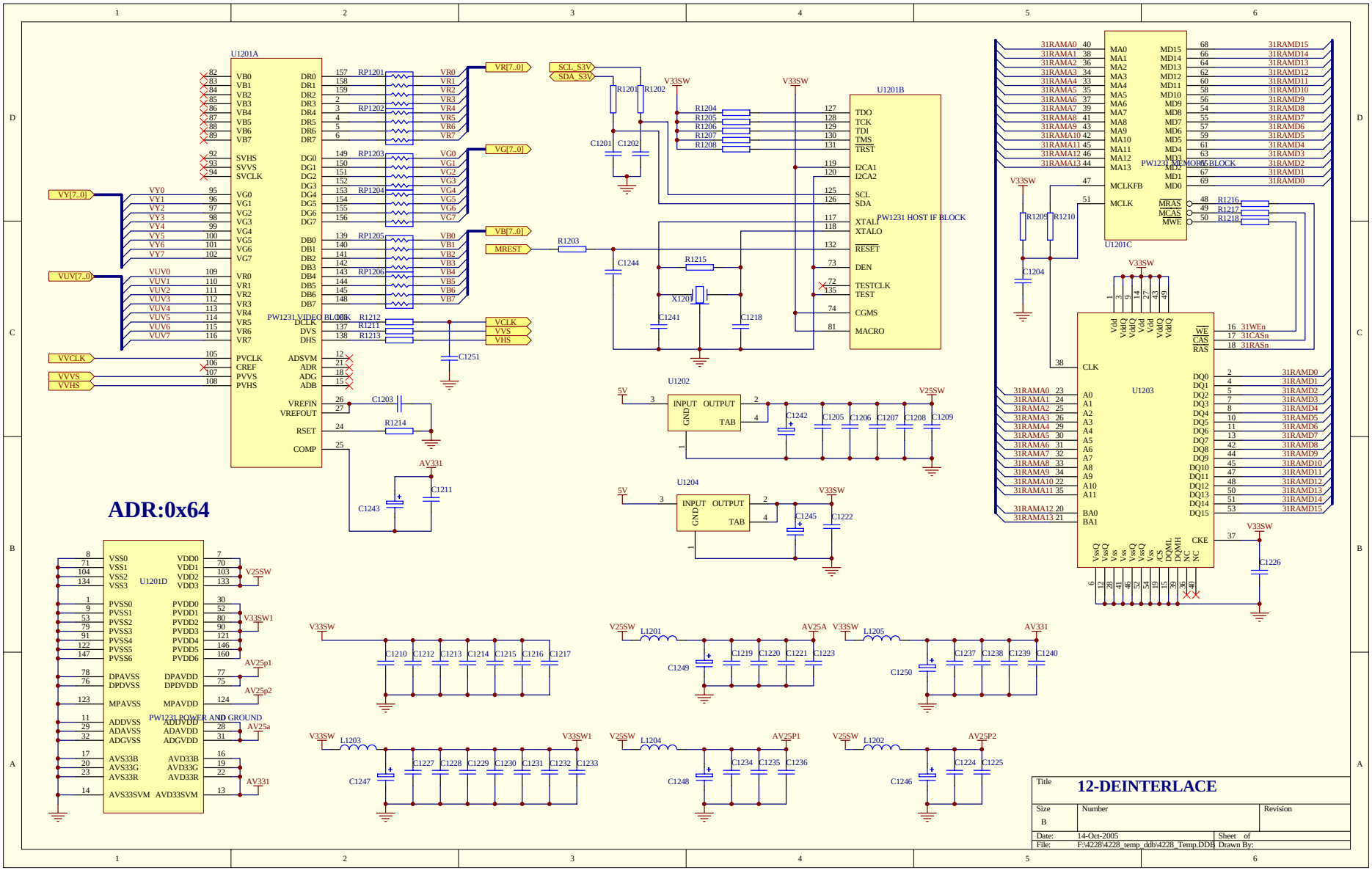
Title	15_TELETEXT_DECODER
Size	B
Number	
Revision	
Date:	14-Oct-2005
Sheet	of
File:	F:\4228\4228_temp_ddb\4228_Temp.DDB
Drawn By:	

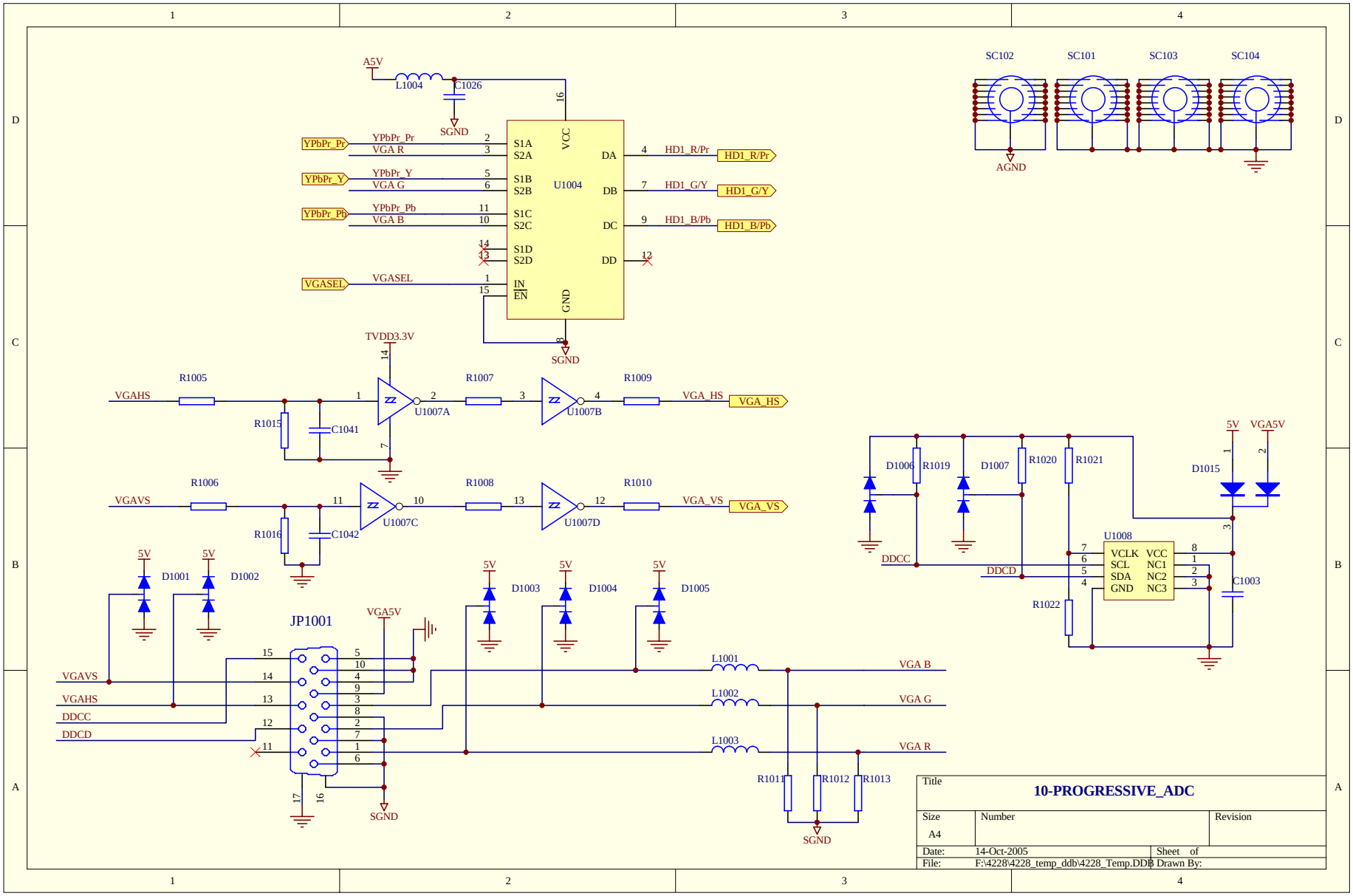

U1102
ADR:0x88
U1101
INPUT
OUTPUT
GND
TAB
5V
VV33
A5V
5VVV
CVBS_O
V_CVBS_M
3230_VO
MREST
SDA_S3V
SCL_S3V
V_AVCVBS
V_TVCVBS
V_SVideo_C
V_SVideo_Y
VYCbCr_Y
VYCbCr_Cb
VYCbCr_Cr
V_TT_G
V_TT_B
V_TT_R
V_TT_FSO
REF_V
#VPEN
VVCLK
VVHS
VVVS
TT_VVHS
TT_VVVS
VY[7..0]
VUV[7..0]
VG[7..0]
VB[7..0]
SGND
Install RP1105~RP1109 if cancel deinterlace IC
Title
11-DECODERV
Size
B
Number
Revision
Date:
14-Oct-2005
Sheet of
File:
F:\4228\4228_temp_ddb\4228_Temp.DDB
Drawn By:

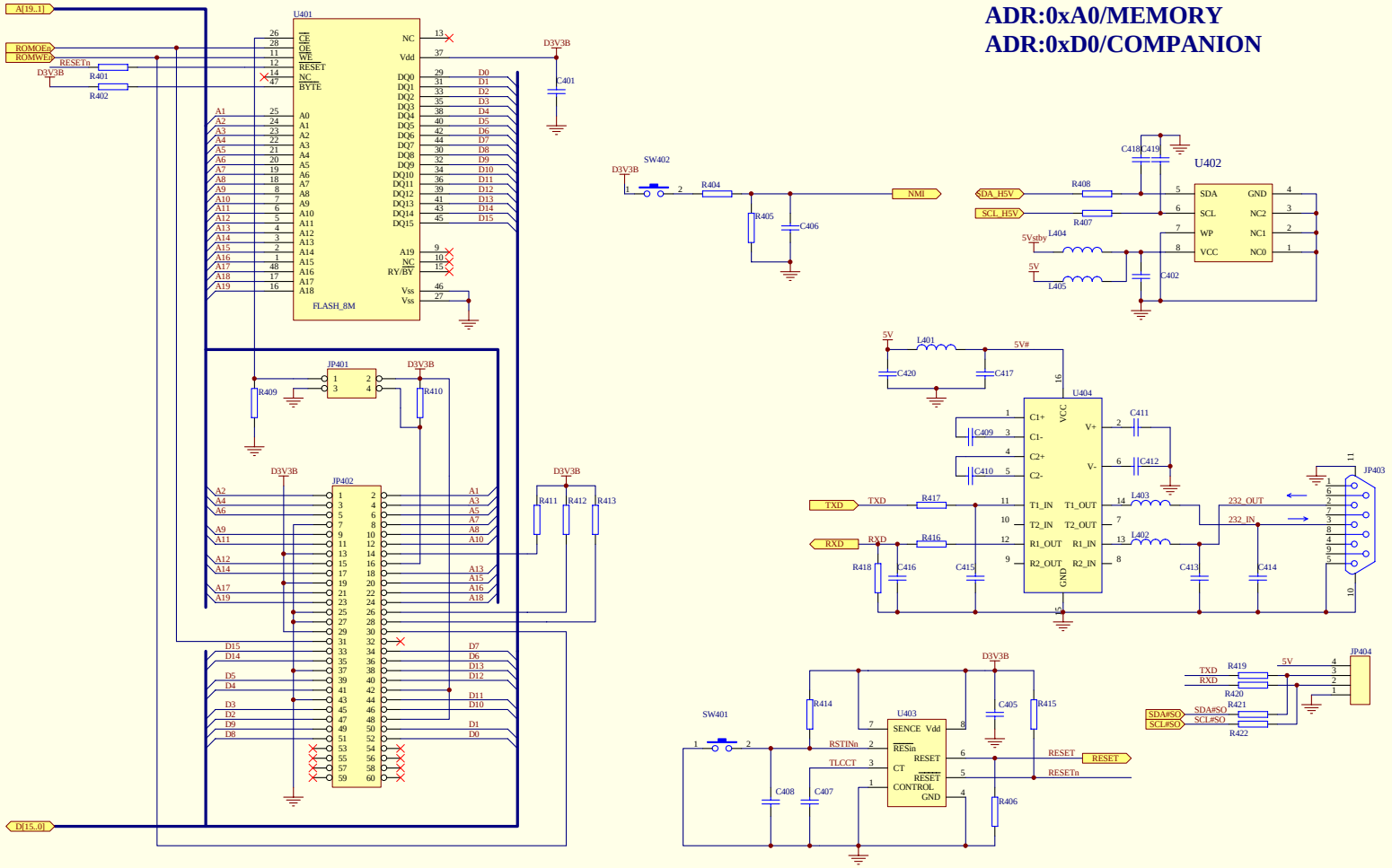

U1402
ADR:0x8E
U1401
INPUT
OUTPUT
GND
TAB
5V
GV33
A5V
5VVG
SGND
MREST
SDA_S3V
SCL_S3V
CVBS_S_O
G_AVCVBS
G_TVCBS
G_SVideo_C
G_SVideo_Y
GYCbCr_Y
GYCbCr_Cb
GYCbCr_Cr
G_TT_G
G_TT_B
G_TT_R
G_TT_FSC
TV_CVBS_S#
TV_CVBS_S
GGE[7..0]
GBE[7..0]
GCLK
GHS
FIELD
GPEN
TT-GHS
GVS
REF_G
X1401
Q1401
Title
14-DECODER_G
Size
B
Number
Revision
Date:
14-Oct-2005
Sheet of
File:
F:\4228\4228_temp_ddb\4228_Temp.DDB
Drawn By:


U803
Vin/INTRO
SDA
SCK
SEN
SMS
HIN
VIDEO
CSYNC
LPF
R
G
B
I2C/SEL
SDO
BOX
VDD
RREF
VSS(A)
TT_VVVS
SDA_S5V
SCL_S5V
5V_V_CCD
TT_VVHS
3230_VO
V_TT_R
V_TT_G
V_TT_B
V_TT_FSO
SGND
A5V
U802
GVS
5V_G_CCD
TT-GHS
TV_CVBS_S
G_TT_R
G_TT_G
G_TT_B
G_TT_FSO
SCL_S3V
SDA_S3V
V33SW
5V
Q801
Q802
L801
L802
Title
8-CCD_DECODER
Size
A4
Number
Revision
Date:
14-Oct-2005
Sheet of
File:
F:\4228\4228_temp_ddb\4228_Temp.DDB
Drawn By:

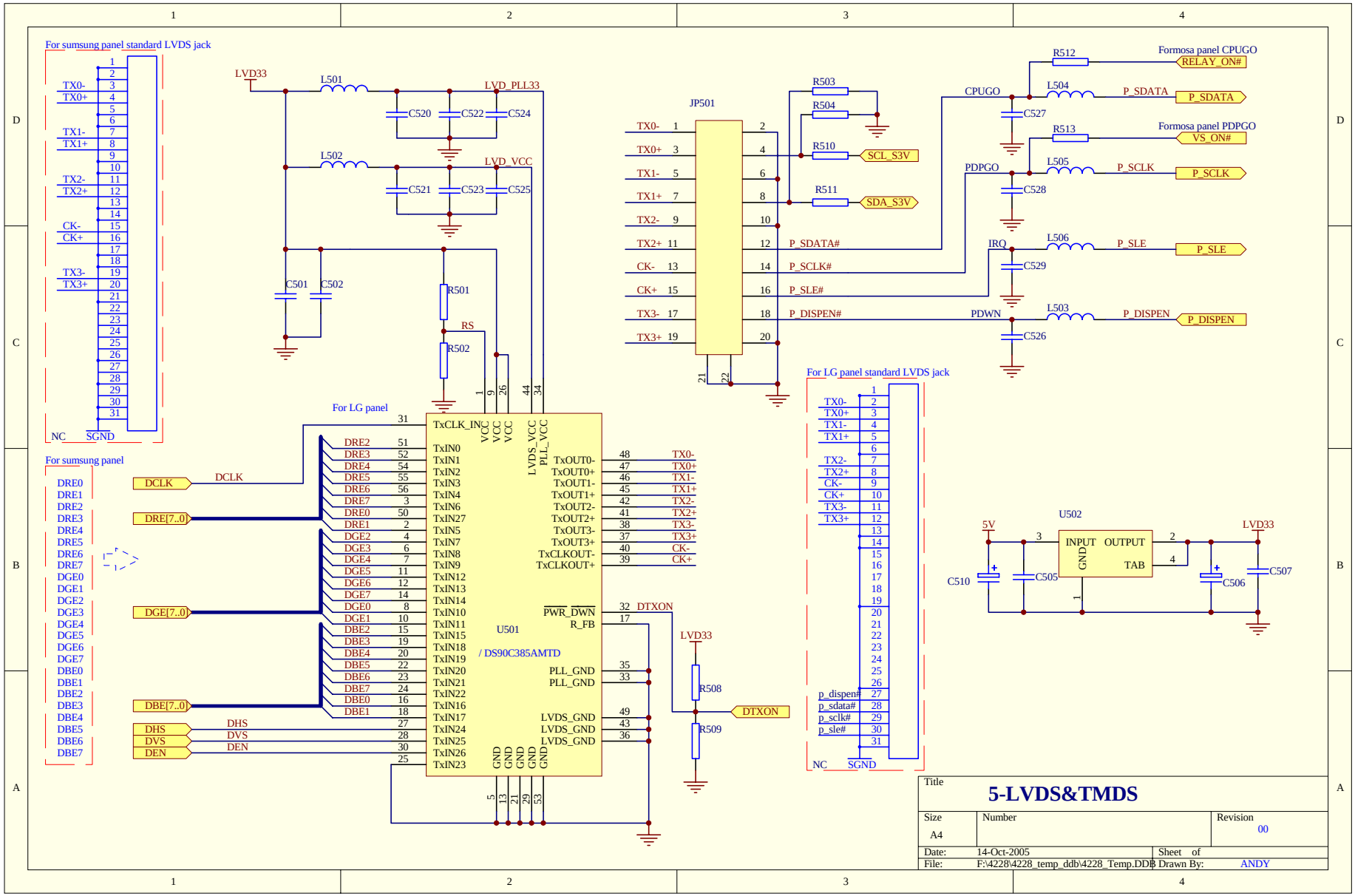

U1301A
PW181 Graphics Port
U1301B
PW181 Video Port
U1301C
U1301D
PW181 MISC
U1301E
PW818 POWER AND GROUND
U1302
U1303
RNMI2
REMARK:
HARDWARE I2C: SDA1 SCL1
SOFTWARE I2C: VSDA VSCL
For Samsung/Formosa panel
2005.05.22
Title
13-SCALER
Size
A3
Number
Revision
Date: 14-Oct-2005
Sheet of
File: F:\4228\4228_temp_ddb\4228_Temp.DDB
Drawn By:


U1201A
PW1231 VIDEO BLOCK
U1201B
PW1231 HOST IF BLOCK
U1201C
PW1231 MEMORY BLOCK
U1201D
PW1231 POWER AND GROUND
U1202
U1203
U1204
ADR:0x64
12-DEINTERLACE
Title
Size
B
Number
Revision
Date: 14-Oct-2005
Sheet of
File: F:\4228\4228_temp_ddb\4228_Temp.DDB
Drawn By:


A5V
L1004
C1026
SGND
U1004
VCC
GND
S1A
S2A
S1B
S2B
S1C
S2C
S1D
S2D
IN
EN
DA
DB
DC
DD
YPbPr_Pr
VGA R
YPbPr_Y
VGA G
YPbPr_Pb
VGA B
VGASEL
HD1_R/Pr
HD1_G/Y
HD1_B/Pb
TVDD3.3V
R1005
R1007
R1009
VGAHS
VGA_HS
U1007A
U1007B
R1015
C1041
R1006
R1008
R1010
VGAVS
VGA_VS
U1007C
U1007D
R1016
C1042
D1001
D1002
D1003
D1004
D1005
JP1001
VGA5V
DDCC
DDCD
L1001
L1002
L1003
VGA B
VGA G
VGA R
R1011
R1012
R1013
SC102
SC101
SC103
SC104
AGND
D1006
R1019
D1007
R1020
R1021
D1015
5V
U1008
VCLK
SCL
SDA
GND
VCC
NC1
NC2
NC3
C1003
R1022
Title
10-PROGRESSIVE_ADC
Size
A4
Number
Revision
Date:
14-Oct-2005
Sheet of
File:
F:\4228\4228_temp_ddb\4228_Temp.DDB
Drawn By:



Title	4-FLASH		
Size	Number		Revision
A3			
Date:	14-Oct-2005	Sheet of	
File:	F:\4228\4228_temp_ddb\4228_Temp.DDB	Drawn By:	


For sumsung panel standard LVDS jack
TX0-
TX0+
TX1-
TX1+
TX2-
TX2+
CK-
CK+
TX3-
TX3+
NC
SGND
LVD33
L501
L502
LVD_PLL33
LVD_VCC
C520
C521
C522
C523
C524
C525
C501
C502
R501
R502
RS
JP501
R503
R504
R510
R511
SCL_S3V
SDA_S3V
P_SDATA#
P_SCLK#
P_SLE#
P_DISPEN#
CPUGO
PDPGO
IRQ
PDWN
R512
R513
L504
L505
L506
L503
C527
C528
C529
C526
Formosa panel CPUGO
RELAY_ON#
Formosa panel PDPGO
VS_ON#
P_SDATA
P_SCLK
P_SLE
P_DISPEN
For LG panel
For sumsung panel
DCLK
DRE[7..0]
DGE[7..0]
DBE[7..0]
DHS
DVS
DEN
TxCLK_IN
TxIN0
TxIN1
TxIN2
TxIN3
TxIN4
TxIN6
TxIN27
TxIN5
TxIN7
TxIN8
TxIN9
TxIN12
TxIN13
TxIN14
TxIN10
TxIN11
TxIN15
TxIN18
TxIN19
TxIN20
TxIN21
TxIN22
TxIN16
TxIN17
TxIN24
TxIN25
TxIN26
TxIN23
U501
/ DS90C385AMTD
VCC
LVDS_VCC
PLL_VCC
GND
TxOUT0-
TxOUT0+
TxOUT1-
TxOUT1+
TxOUT2-
TxOUT2+
TxOUT3-
TxOUT3+
TxCLKOUT-
TxCLKOUT+
PWR_DWN
R_FB
PLL_GND
LVDS_GND
DTXON
R508
R509
For LG panel standard LVDS jack
p_dispen#
p_sdata#
p_sclk#
p_sle#
U502
5V
INPUT
OUTPUT
GND
TAB
C510
C505
C506
C507
Title
5-LVDS&TMDS
Size
A4
Number
Revision
00
Date:
14-Oct-2005
Sheet of
File:
F:\4228\4228_temp_ddb\4228_Temp.DDB
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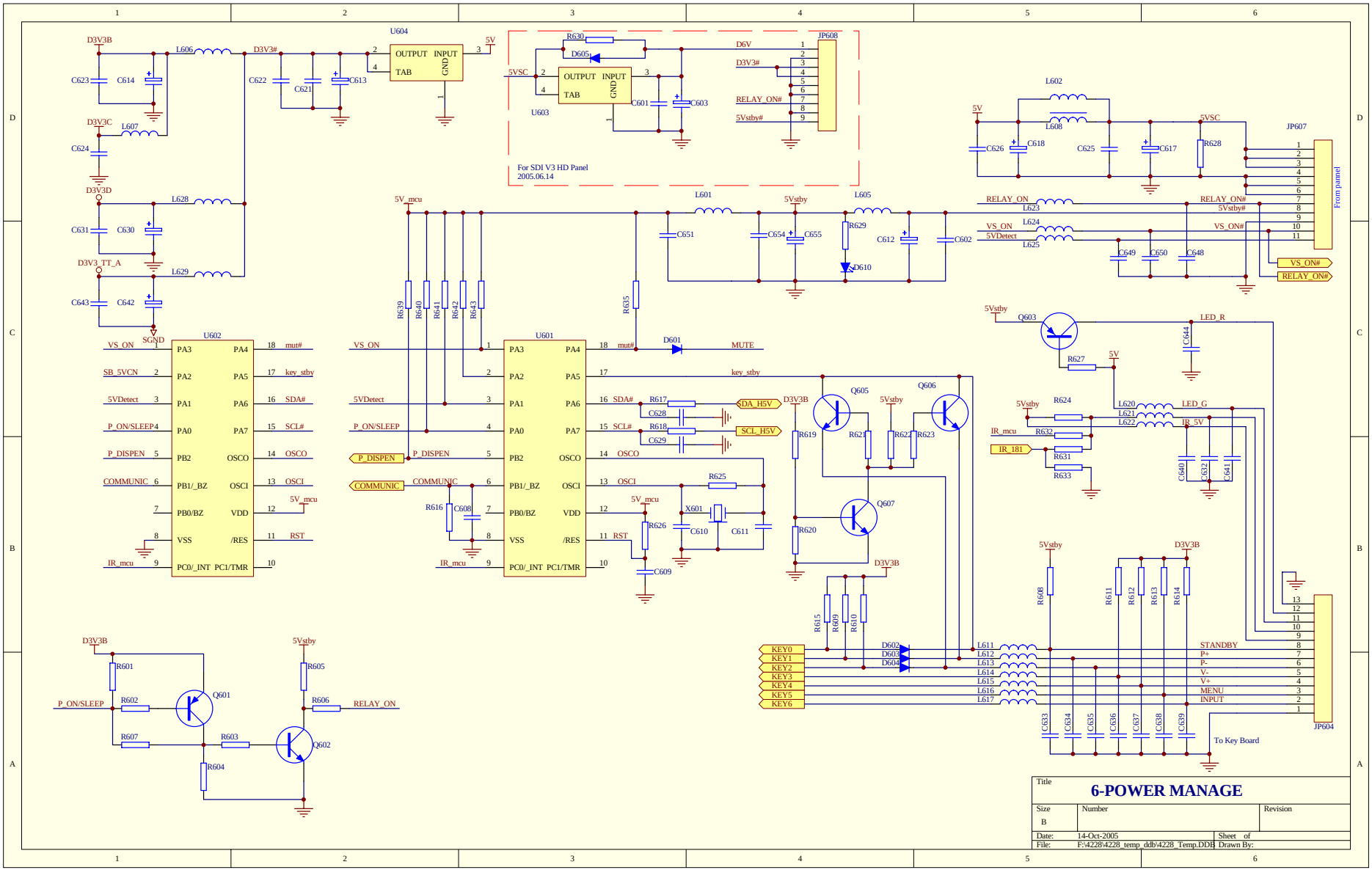
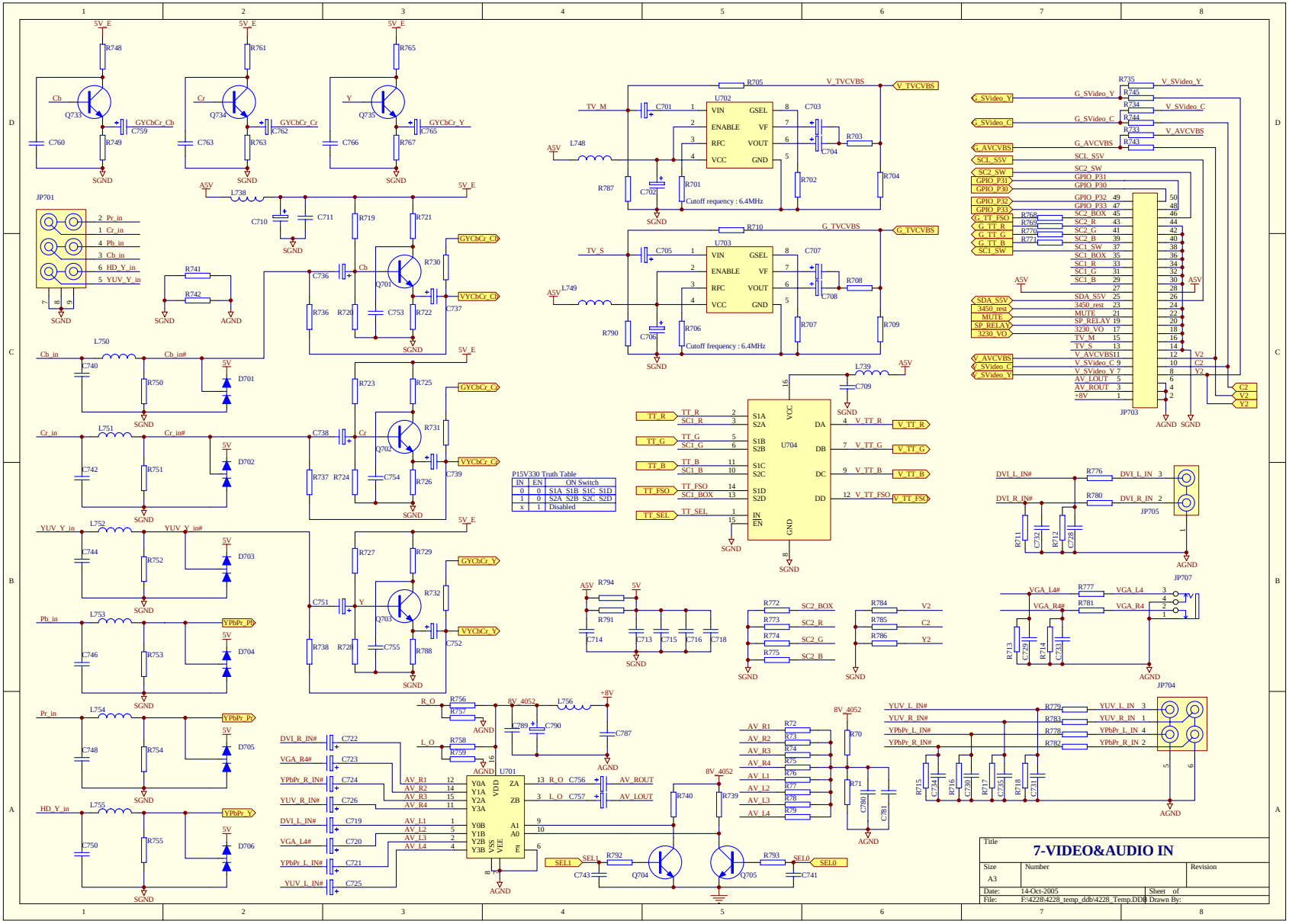
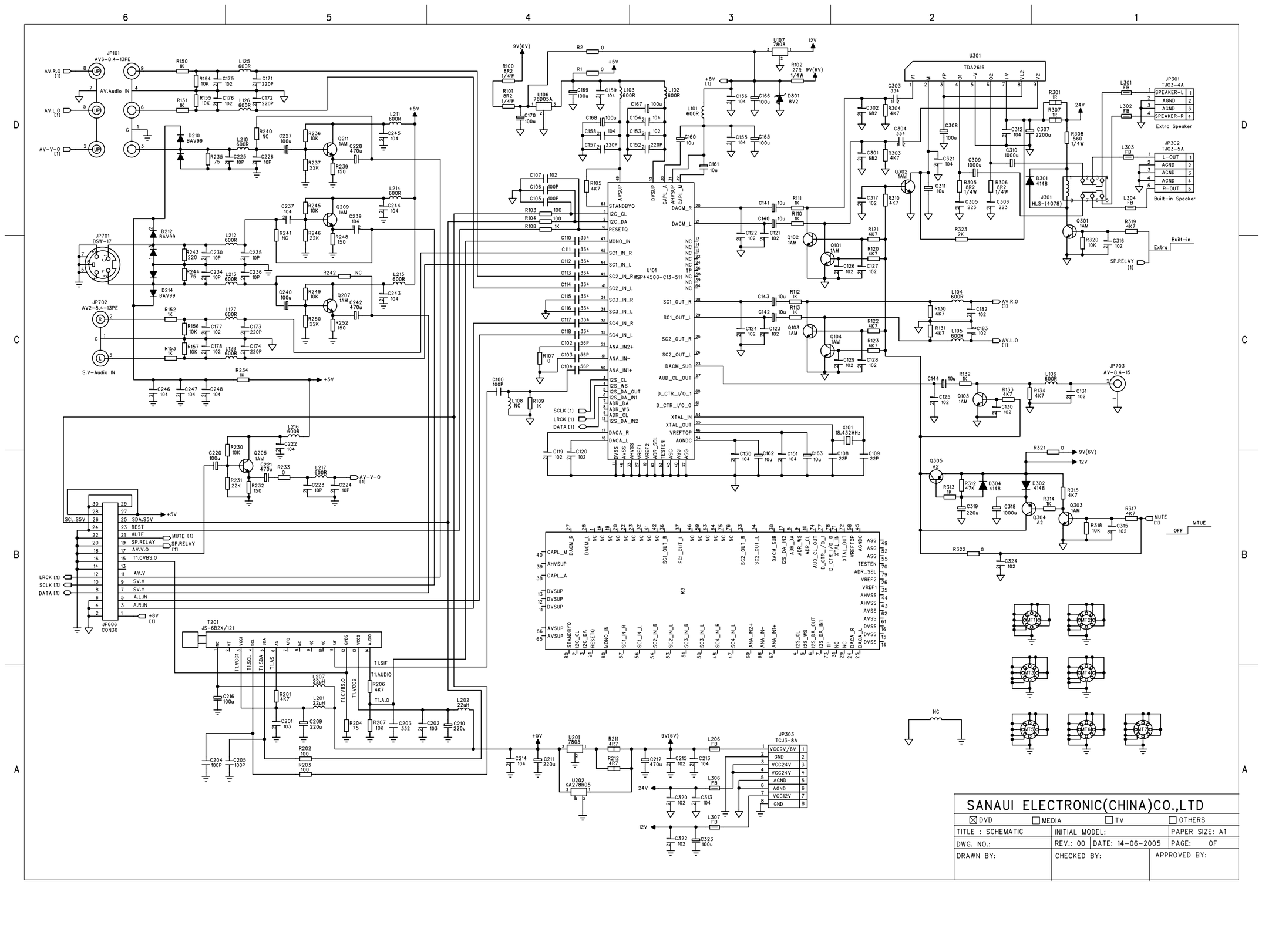
ANDY

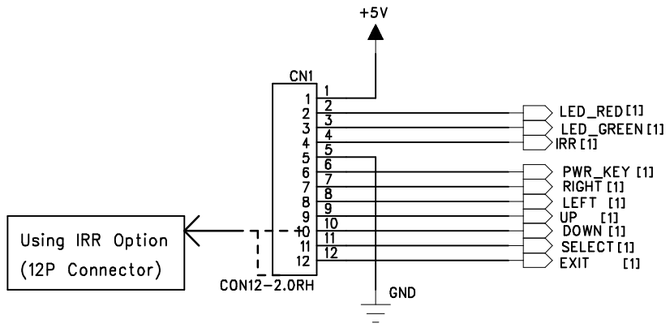

U604
OUTPUT INPUT
TAB GND
U603
JP608
For SDI V3 HD Panel
2005.06.14
U602
U601
PA3 PA4 PA5 PA6 PA1 PA0 PB2 PB1/_BZ PB0/BZ VSS PC0/_INT PA7 OSCO OSCI VDD /RES PC1/TMR
JP607
From pannel
JP604
To Key Board
Q601
Q602
Q603
Q605
Q606
Q607
Title
6-POWER MANAGE
Size
B
Number
Revision
Date: 14-Oct-2005
Sheet of
File: F:\4228\4228_temp_ddb\4228_Temp.DDB
Drawn By:

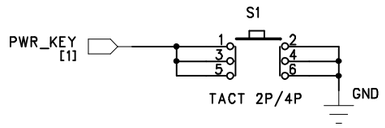

7-VIDEO&AUDIO IN
Size A3
Number
Revision
Date: 14-Oct-2005
Sheet of
File: F:\4228\4228_temp_ddb\4228_Temp.DDB
Drawn By:
P15V330 Truth Table
IN | EN | ON Switch
0 | 0 | S1A S1B S1C S1D
1 | 0 | S2A S2B S2C S2D
x | 1 | Disabled
Cutoff requency : 6.4MHz
Cutoff frequency : 6.4MHz
JP701
JP703
JP704
JP705
JP707
U702
U703
U704
U701

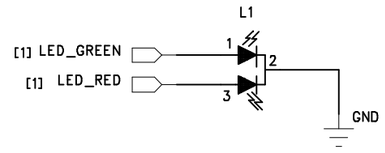

JP101 AV6-8.4-13PE
AV.R.O [1]
AV.Audio IN
AV.L.O [1]
AV-V-O [1]
JP701 DSW-17
JP702 AV2-8.4-13PE
S.V-Audio IN
U101 MSP4450G-C13-511
STANDBYQ
I2C_CL
I2C_DA
RESETQ
MONO_IN
SC1_IN_R
SC1_IN_L
SC2_IN_R
SC2_IN_L
SC3_IN_R
SC3_IN_L
SC4_IN_R
SC4_IN_L
ANA_IN2+
ANA_IN-
ANA_IN1+
I2S_CL
I2S_WS
I2S_DA_OUT
I2S_DA_IN1
I2S_DA_IN2
ADR_DA
ADR_WS
ADR_CL
SCLK [1]
LRCK [1]
DATA [1]
DACA_R
DACA_L
SC1_OUT_R
SC1_OUT_L
SC2_OUT_R
SC2_OUT_L
DACM_SUB
AUD_CL_OUT
D_CTR_I/O_1
D_CTR_I/O_0
XTAL_IN
XTAL_OUT
VREFTOP
AGNDC
U107 7808
U106 78D05A
U201 7805
U202 KA278R05
U301 TDA2616
X101 18.432MHz
JP301 TJC3-4A
Extra Speaker
JP302 TJC3-5A
Built-in Speaker
JP303 TJC3-8A
JP606 CON30
T201 JS-6B2X/121
J301 HLS-(4078)
Built-in Extra
SP.RELAY [1]
MUTE [1]
OFF
MTUE
SANAUI ELECTRONIC(CHINA)CO.,LTD
TITLE : SCHEMATIC
INITIAL MODEL:
PAPER SIZE: A1
DWG. NO.:
REV.: 00
DATE: 14-06-2005
PAGE: OF
DRAWN BY:
CHECKED BY:
APPROVED BY:

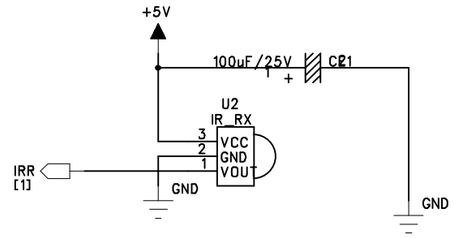
DUBHE OSD

6-Key OSD

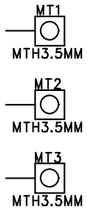


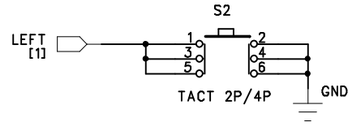


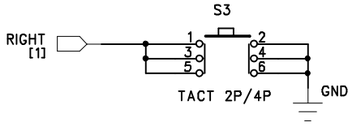


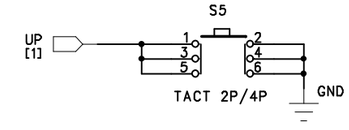


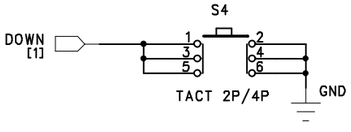
OSD I/F Connector

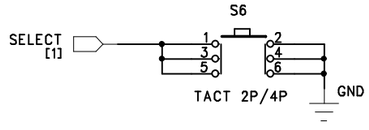


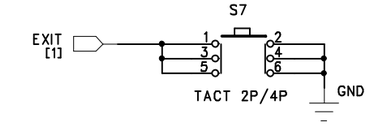






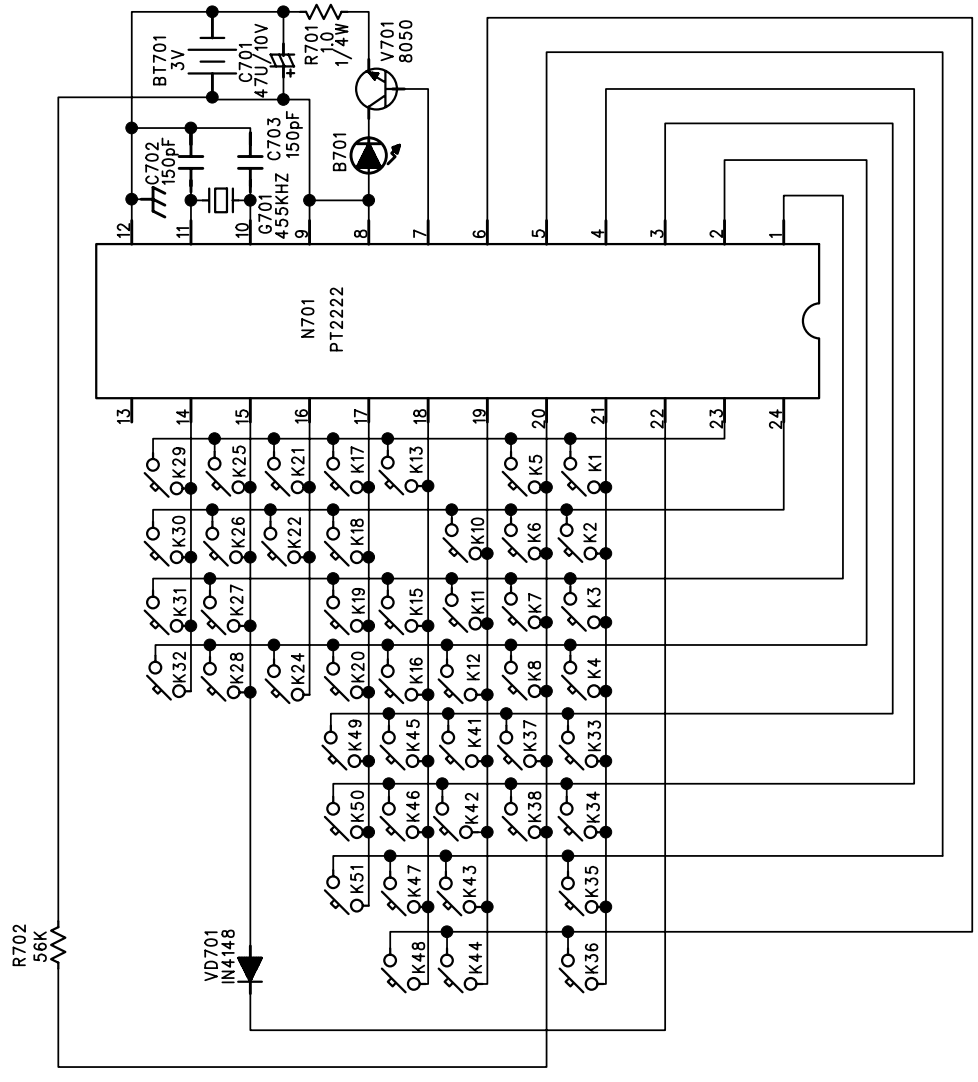






	Project: Project Name	Rev: 1.2
	Title: DUBHE OSD	
	Date: June. 15,2004	Sheet: xx of xx

REMOTE PCB



REMOTE CONTROL CODE ASSIGNMENT

KEY NO.	KEY NAME	DATA CODE	KEY NO.	KEY NAME	DATA CODE
K1	POWER	00	K33	dumb	40
K2	1	01	K34	dumb	41
K3	2	02	K35	dumb	42
K4	3	03	K36	dumb	43
K5	P.MODE	04	K37	MUTE	44
K6	4	05	K38	INFO	45
K7	5	06	K39	nil	46
K8	6	07	K40	nil	47
K9	nil	08	K41	100	48
K10	7	09	K42	PREV	49
K11	8	0A	K43	P.STILL	4A
K12	9	0B	K44	SOUND	4B
K13	MTS	0C	K45	SLEEP	4C
K14	nil	0D	K46	TIME	4D
K15	S.SELE	0E	K47	Picture	4E
K16	OK	0F	K48	CH Erase	4F
K17	CH.+	10	K49	CH Save	50
K18	VOL.+	11	K50	C/C	51
K19	VOL.-	12	K51	V-CHIP	52
K20	CH.-	13	K52	nil	53
K21	MENU	14	K53	nil	54
K22	Source	15	K54	nil	55
K23	nil	16	K55	nil	56
K24	P.SIZE	17	K56	nil	57
K25	0	18	K57	nil	58
K26	F.White	19	K58	nil	59
K27	PIP Source	1A	K59	nil	5A
K28	EXIT	1B	K60	nil	5B
K29	PIP	1C	K61	nil	5C
K30	SWAP	1D	K62	nil	5D
K31	PIP CH-	1E	K63	nil	5E
K32	PIP CH+	1F	K64	nil	5F

CUSTOM CODE: 20DD

FOR NTSC

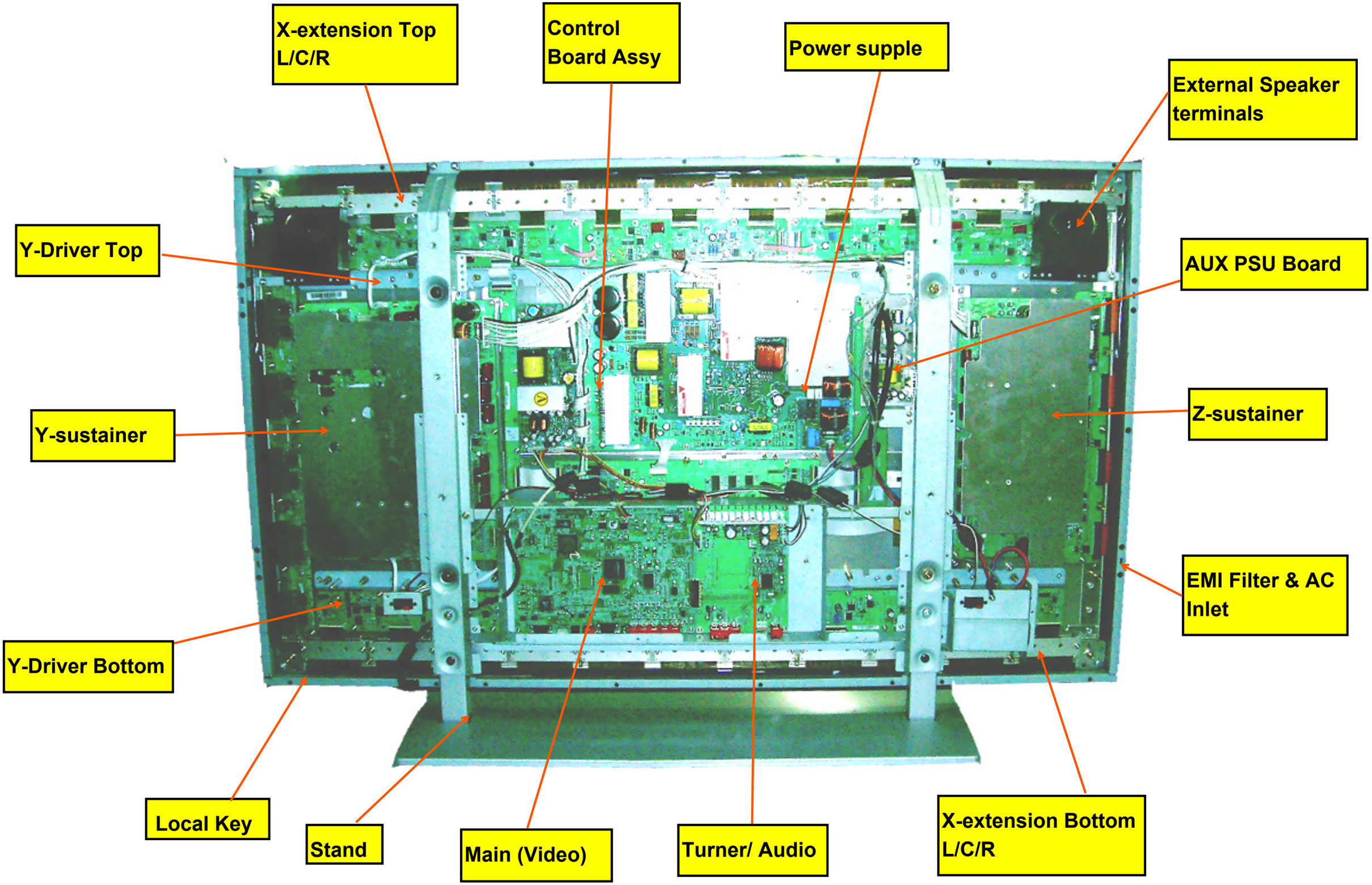
Basic Operations & Circuit Description

MODULE

There are 1 pc. panel and 12 pc.s PCB including 2 pc.s Y/Z Sustainer board, 2 pc.s Y Drive board, 6 pc.s X Extension boards, 1 pc. Control (Signal Input) and 1 pc. Power board in the Module.

SET

There are 6 pc.s PCBs including 1 pc. AUX. PSU Board, 1 pc. Keypad board, 1 pc. Remote Control Receiver board, 1 pc. L/R Speakers and 1 pc. Main (Video) board in the SET.


X-extension Top L/C/R
Control Board Assy
Power supple
External Speaker terminals
Y-Driver Top
AUX PSU Board
Y-sustainer
Z-sustainer
EMI Filter & AC Inlet
Y-Driver Bottom
Local Key
Stand
Main (Video)
Turner/ Audio
X-extension Bottom L/C/R

PCB function

1. **Power:**
   (1). Input voltage: AC 100V~120V, 45Hz~60Hz.
   Input range: AC 90V(Min)~265V(Max) auto regulation.
   (2). To provide power for PCBs.
2. **Main (Video InterFace) board: To converter TV signals, S signals, AV signals, Y Pb/Cb Pr/Cr signals, DVI signals and D-SUB signals to digital ones and to transmit to Control board.**
3. **Control board: Dealing with the digital signal for output to panel.**
4. **Y-Sustainer / Z-Sustainer board:**
   (1). Receiving the signals from Control and high voltage supply.
   (2). Output scanning waveform for Module.
5. **Y-Drive board: Receive signal from Y sustainer, output horizontal scanning wave-form to the panel.**
6. **X extension board (6pcs): Output addressing signals.**
7. **Tuner/Audio Board：Process and Amplifying the audio signal to speakers and convert TV RF signal to video/audio signal and send to Main board.**

PCB failure analysis

1. **CONTROL : a. Abnormal noise on screen. b. No picture.**
2. **MAIN (video) : a. Lacking color, Bad color scale.**
   b. No voice.
   c. No picture but with signals output, OSD and back light.
   d. Abnormal noise on screen.
3. **POWER : No picture, no power output.**
4. **Z - Sustainer : a. No picture.**
   b. Color not enough.
   c. Flash on screen.
5. **Y - Sustainer : Darker picture with signals.**

6. **X - Extension : Abormal vertical noise on screen.**
7. **Audio Board or AUX PSU: a. No voice. (Make sure Mute/OFF) .**
   b. Noise.

Basic operation of Plasma Display

1. After turning on power switch, power board sends 5Vst-by Volt to Micro Processor

2. The micro Processor memorize the last state of Power, When the last state of power is on or receive power on signal from local Key or Remote control, Micro Processor will send on control signal to power. Then Power sends (5Vsc, 9Vsc, 24V and RLYON, Vs ON) to PCBs working. This time VIF will send signals to display Image, OSD on the panel and start to search available signal sources.
   If the audio signals input, them will be amplified by Audio AMP and transmitted to Speakers.

3. If some abnormal signals are detected (for example: over volts, over current, over temperature and under volts), the system will be shut down by Power off.

Main IC Specifications

- PW181 Image Processor, Scaler
- PW1231 Digital Video Signal Processor
- VPC 323XD Comb-filter Video Processor
- Z86229 NTSC Line 21 CCD decorder
- MSP34x0G Multistandard Sound Processor
-AD9880 Analog/HDMI Dual Display Interface
-PI5V330 Wideband/Video Quad 2-Channel MUX/DEMUX
-SM5304AV Video Buffer with Built-in Analog LPF
-TDA2616 2 X 12 W hi-fi audio power amplifier with mute
-SAA5360 Multi page intelligent teletext decoder
-AT24C32 Z-Wire Serial EEPROM
-HT48R06A-1 8-Bit Cost-Effective I/O Type MCU

PW181

Product Specification

General Description

The PW181 ImageProcessor is a highly integrated "system-on-a-chip" that interfaces computer graphics and video inputs in virtually any format to a fixed-frequency flat panel display.

Computer and video images from NTSC/PAL to WUXGA at virtually any refresh rate can be resized to fit on a fixed-frequency target display device with any resolution up to WUXGA. Video data from 4:3 aspect ratio NTSC or PAL and 16:9 aspect ratio HDTV or SDTV is supported. Multi-region, nonlinear scaling allows these inputs to be resized optimally for the native resolution of the display.

Advanced scaling techniques are supported, such as format conversion using multiple programmable regions. Three independent image scalers coupled with frame locking circuitry and dual programmable color lookup tables create sharp images in multiple windows, without user intervention.

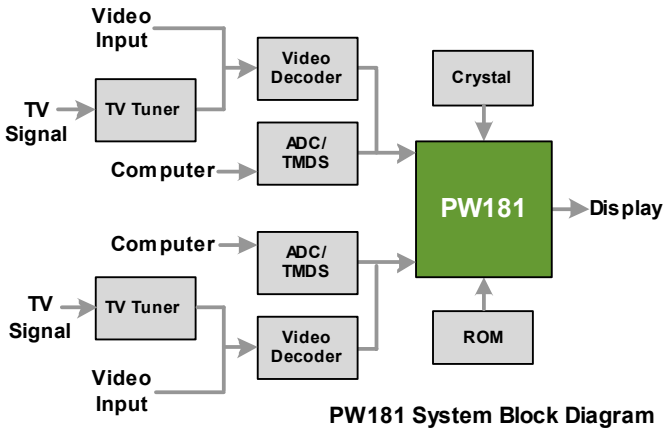
Embedded SDRAM frame buffers and memory controllers perform frame rate conversion and enhanced video processing completely on-chip. A separate memory is dedicated to storage of on-screen display images and CPU general purpose use.

Advanced video processing techniques are supported using the internal frame buffer, including motion adaptive, temporal deinterlacing with film mode detection. When used in combination with the new third-generation scaler, this advanced video processing technology delivers the highest quality video for advanced displays.

Both input ports support integrated DVI 1.0 content protection using standard DVI receivers.

A new advanced OSD Generator with more colors and larger sizes supports more demanding OSD applications, such as on-screen programming guides. When coupled with the new, faster, integrated microprocessor, this OSD Generator supports advanced OSD animation techniques.

Programmable features include the user interface, custom start-up screen, all automatic imaging features, and special screen effects.



PW181 System Block Diagram

Features

- Third-generation, two-dimensional filtering techniques
- Third-generation, advanced scaling techniques
- Second-generation Automatic Image Optimization
- Frame rate conversion
- Video processing
- On-Screen Display (OSD)
- On-chip microprocessor
- JTAG debugger and boundary scan
- Picture-in-picture (PIP)
- Multi-region, non-linear scaling
- Hardware 2-wire serial bus support

Applications

- Multimedia Displays
- Plasma Displays
- Digital Television

Device	Application	Package
PW181-10V	Up to XGA Displays	352 PBGA
PW181-20V	Up to UXGA Displays	

pixelworks

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www.pixelworks.com

PRELIMINARY / CONFIDENTIAL

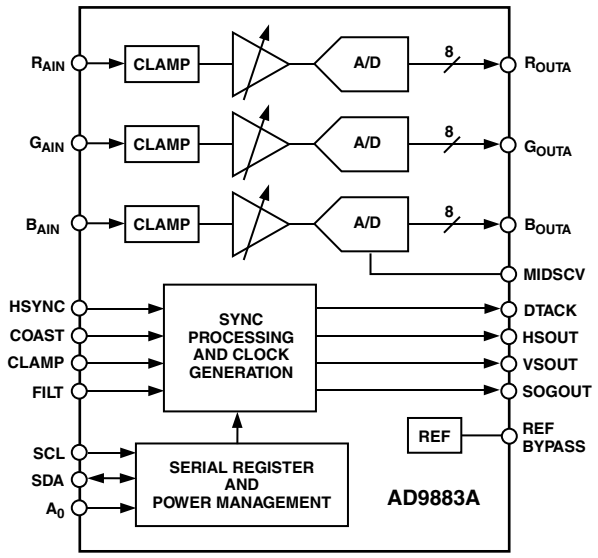
110 MSPS/140 MSPS Analog Interface for Flat Panel Displays

AD9883A

FEATURES
140 MSPS Maximum Conversion Rate
300 MHz Analog Bandwidth
0.5 V to 1.0 V Analog Input Range
500 ps p-p PLL Clock Jitter at 110 MSPS
3.3 V Power Supply
Full Sync Processing
Sync Detect for "Hot Plugging"
Midscale Clamping
Power-Down Mode
Low Power: 500 mW Typical
4:2:2 Output Format Mode

APPLICATIONS
RGB Graphics Processing
LCD Monitors and Projectors
Plasma Display Panels
Scan Converters
Microdisplays
Digital TV

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9883A is a complete 8-bit, 140 MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 140 MSPS encode rate capability and full power analog bandwidth of 300 MHz supports resolutions up to SXGA (1280 × 1024 at 75 Hz).

The AD9883A includes a 140 MHz triple ADC with internal 1.25 V reference, a PLL, and programmable gain, offset, and clamp control. The user provides only a 3.3 V power supply, analog input, and Hsync and COAST signals. Three-state CMOS outputs may be powered from 2.5 V to 3.3 V.

The AD9883A's on-chip PLL generates a pixel clock from the Hsync input. Pixel clock output frequencies range from 12 MHz to 140 MHz. PLL clock jitter is 500 ps p-p typical at 140 MSPS. When the COAST signal is presented, the PLL maintains its output frequency in the absence of Hsync. A sampling phase adjustment is provided. Data, Hsync, and clock output phase relationships are maintained. The AD9883A also offers full sync processing for composite sync and sync-on-green applications.

A clamp signal is generated internally or may be provided by the user through the CLAMP input pin. This interface is fully programmable via a 2-wire serial interface.

Fabricated in an advanced CMOS process, the AD9883A is provided in a space-saving 80-lead LQFP surface-mount plastic package and is specified over the 0°C to 70°C temperature range.

REV. A

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Tel:
Fax:

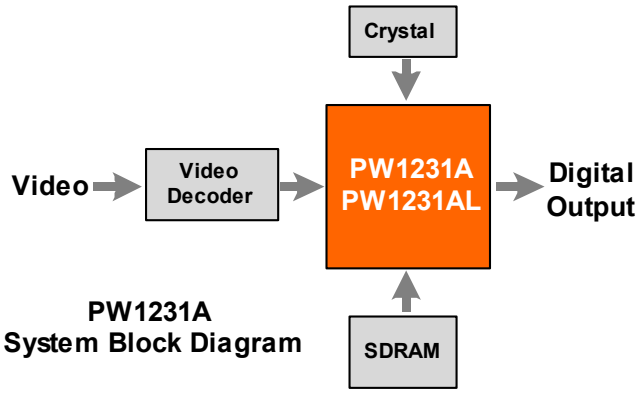
PW1231A

Product Specification

General

The PW1231A is a high-quality, digital video signal processor that incorporates Pixelworks' patented deinterlacing, scaling, and video enhancement algorithms. The PW1231A accepts industry-standard video formats and resolutions, and converts the input into many desired output formats.The highly efficient video algorithms result in excellent quality video.

The PW1231A combines many functions into a single device, including a memory controller, auto-configuration, and others. This high level of integration enables simple, flexible, cost-effective solutions that require fewer components.



PW1231A
System Block Diagram

Features

- Built-In Memory Controller
- Motion-Adaptive Deinterlace Processor
- Intelligent Edge Deinterlacing
- Digital Color/Luminance Transient Improvement (DCTI/DLTI)
- Interlaced Video Input Options, including NTSC and PAL
- Independent horizontal and vertical scaling
- Copy Protection
- Two-Wire Serial Interface

Applications:
For use with Digital Displays

- Flat-Panel (LCD, DLP) TVs
- Rear Projection TVs
- Plasma Displays
- LCD Multimedia Monitors
- Multimedia Projectors

Device	Application	Package
PW1231A PW1231AL	Up to XGA	160-pin PQF

NOTE: "L" denotes lead (Pb) free

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www.pixelworks.com

P/N 001-0097-00 Rev B
July 2003

PRELIMINARY—CONFIDENTIAL

Analog/HDMI Dual Display Interface

Preliminary Datasheet 3/26/2004 AD9880

FEATURES

- **Analog/HDMI Dual Interface**
- **Supports High-Bandwidth Digital Content Protection**
- **RGB to YCbCr two-way color conversion**
- **Automated clamping level adjustment**
- **1.8/3.3V Power Supply**
- **100-pin LQFP Pb-Free Package**
- **RGB and YCbCr Output Formats**

Analog Interface

- **8-bit Triple Analog to Digital Converters**
- **150 MSPS Maximum Conversion Rate**
- **Macrovision Detection**
- **2:1 Input Mux**
- **Full Sync Processing**
- **Sync Detect for "Hot Plugging"**
- **Mid-Scale Clamping**

Digital Video Interface

- **HDMI 1.0, DVI 1.0**
- **150 MHz HDMI Receiver**
- **Supports High-Bandwidth Digital Content Protection (HDCP 1.1)**

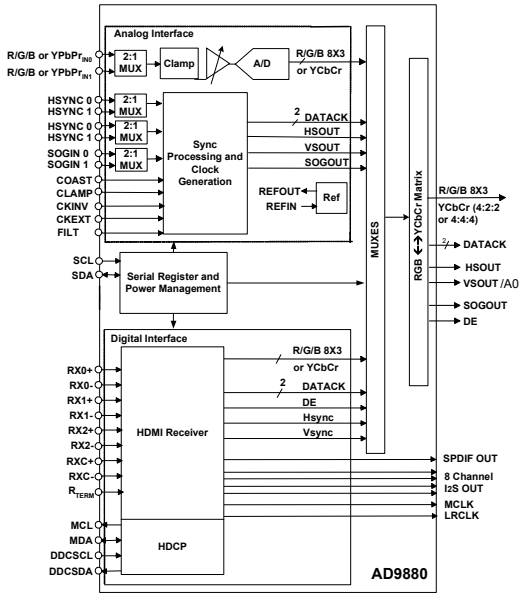
Digital Audio Interface

- **HDMI 1.0 compatible audio interface**
- **S/PDIF (IEC90658 compatible) digital audio output**
- **Multi-channel I^2S audio output (up to 8 channels)**

APPLICATIONS

- **Advanced TV**
- **HDTV**
- **Projectors**
- **LCD Monitor**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9880 offers designers the flexibility of an analog interface and High-Definition Multimedia Interface (HDMI) receiver integrated on a single chip. Also included is support for High bandwidth Digital Content Protection (HDCP).

Analog Interface

The AD9880 is a complete 8-bit 150 MSPS monolithic analog interface optimized for capturing Component Video (YPbPr) and RGB graphics signals. Its 150 MSPS encode rate capability and full power analog bandwidth of 300 MHz supports all HDTV formats (up to 1080p) and FPD resolutions up to SXGA (1280 x 1024 at 75 Hz).

The analog interface includes a 150 MHz triple ADC with internal 1.25V reference, a Phase Locked Loop (PLL), and programmable gain, offset, and clamp control. The user provides only 1.8V and 3.3V power supply, analog input, and Hsync. Three-state CMOS outputs may be powered from 1.8V to 3.3V. The AD9880's on-chip PLL generates a pixel clock from Hsync. Pixel clock output frequencies range from 12 MHz to 150 MHz. PLL clock jitter is typically less than 500 ps p-p at 150 MHz. The AD9880 also offers full sync processing for composite sync and Sync-on-Green (SOG) applications.

Digital Interface

The AD9880 contains a HDMI 1.0 compatible receiver and supports all HDTV formats (up to 1080p) and display resolutions up to SXGA (1280 x 1024 at 75 Hz). The receiver features an intra-pair skew tolerance of up to one full clock cycle. With the inclusion of HDCP, displays may now receive encrypted video content. The AD9880 allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission as specified by the HDCP 1.1 protocol.

Fabricated in an advanced CMOS process, the AD9880 is provided in a space-saving 100-lead LQFP surface-mount plastic package and is specified over the 0 ºC to 70 ºC temperature range.

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Comb Filter Video Processor

1. Introduction

The VPC 323xD is a high-quality, single-chip video front-end, which is targeted for 4:3 and 16:9, 50/60-Hz and 100/120 Hz TV sets. It can be combined with other members of the DIGIT3000 IC family (such as DDP 331x) and/or it can be used with 3rd-party products.

The main features of the VPC 323xD are

- high-performance adaptive 4H comb filter Y/C separator with adjustable vertical peaking
- multi-standard color decoder PAL/NTSC/SECAM including all substandards
- four CVBS, one S-VHS input, one CVBS output
- two RGB/YC_rC_b component inputs, one Fast Blank (FB) input
- integrated high-quality A/D converters and associated clamp and AGC circuits
- multi-standard sync processing
- linear horizontal scaling (0.25 ... 4), as well as non-linear horizontal scaling ‘Panoramavision’
- PAL+ preprocessing
- line-locked clock, data and sync, or 656-output interface
- peaking, contrast, brightness, color saturation and tint for RGB/YC_rC_b and CVBS/S-VHS
- high-quality soft mixer controlled by Fast Blank
- PIP processing for four picture sizes ($\frac{1}{4}$, $\frac{1}{9}$, $\frac{1}{16}$, or $\frac{1}{36}$ of normal size) with 8-bit resolution
- 15 predefined PIP display configurations and expert mode (fully programmable)
- control interface for external field memory
- I^2C-bus interface
- one 20.25-MHz crystal, few external components
- 80-pin PQFP package

1.1. System Architecture

Fig.1–1 shows the block diagram of the video processor

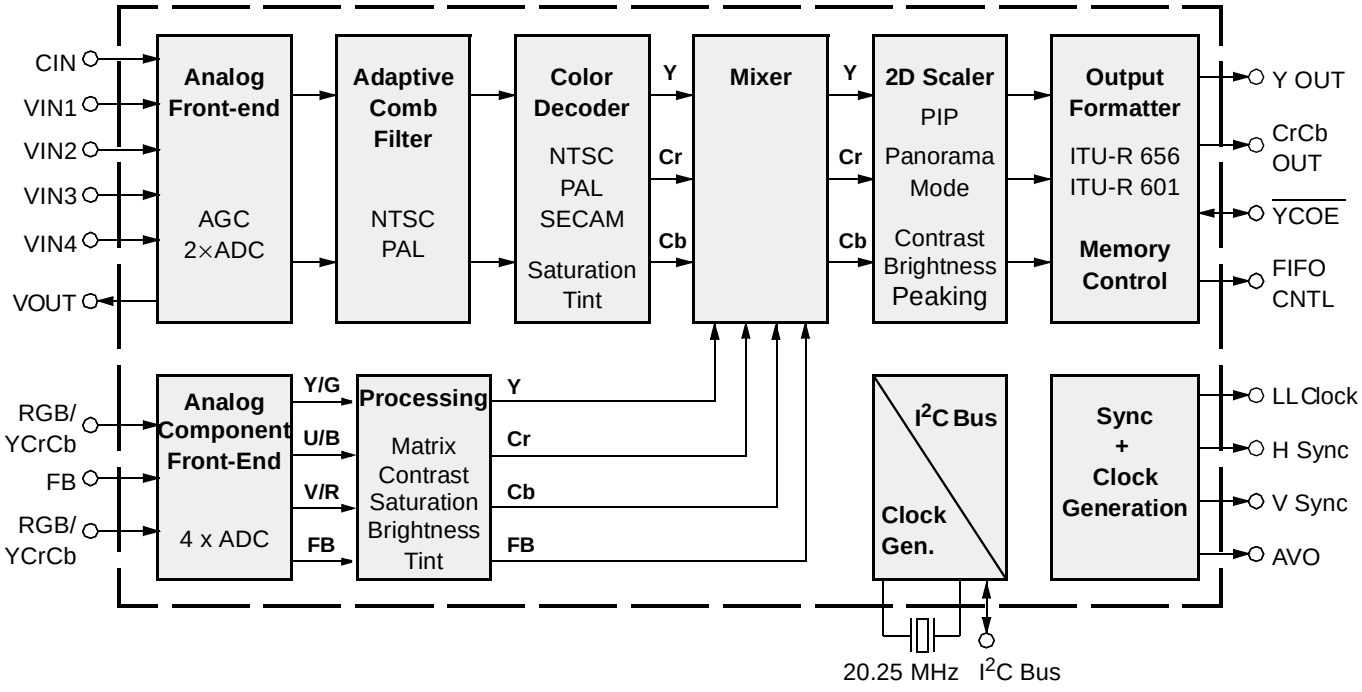


Fig. 1–1: Block diagram of the VPC 323xD

ZiLOG

Totally Logical

Z86229

NTSC LINE 21 CCD DECODER

FEATURES

Devices	Speed (MHz)	Pin Count/ Package Types	Standard Temp. Range	On-Screen Display & Closed Captioning	Automatic Data Extraction: Program Rating	Automatic Data Extraction: Time of Day
Z86229	12	18-Pin DIP, SOIC	0°C to +70°C	Yes	Yes	Yes

- Complete Stand-Alone Line 21 Decoder for Closed-Captioned and Extended Data Services (XDS)
- Preprogrammed to Provide Full Compliance with EIA–608 Specifications for Extended Data Services
- Automatic Extraction and Serial Output of Special XDS Packets (Time of Day, Local Time Zone, and Program Blocking)
- Programmable XDS Filter for a Specific XDS Packet
- Cost-Effective Solution for NTSC Violence Blocking inside Picture-in-Picture (PiP) Windows
- Minimal Communications and Control Overhead Provide Simple Implementation of Violence Blocking, Closed Captioning, and Auto Clock Set Features
- Programmable, On-Screen Display (OSD) for Creating Full Screen OSD or Captions inside a Picture-in-Picture (PiP) Window
- User-Programmable Horizontal Display Position for easy OSD Centering and Adjustment
- I^2C Serial Data and Control Communication
- Supports 2 Selectable I^2C Addresses

GENERAL DESCRIPTION

Capable of processing Vertical Blanking Interval (VBI) data from both fields of the video frame in data, the Z86229 Line 21 Decoder offers a feature-rich solution for any television or set-top application. The robust nature of the Z86229 helps the device conform to the transmission format defined in the Television Decoder Circuits Act of 1990, and in accordance with the Electronics Industry Association specification 608 (EIA–608).

The Line 21 data stream can consist of data from several data channels multiplexed together. Field 1 consists of four data channels: two Captions and two Texts. Field 2 consists of five additional data channels: two Captions, two Texts, and Extended Data Services (XDS). The XDS data structure is defined in EIA–608. The Z86229 can recover and display data transmitted on any of these nine data channels.

The Z86229 can recover and output to a host processor via the I^2C serial bus. The recovered XDS data packet is further defined in the EIA–608 specification. The on-chip XDS filters in the Z86229 are fully programmable, enabling recovery of only those XDS data packets selected by the user. This functionality allows the device to extract the required XDS information with proper XDS filter setup for compatibility in a variety of TVs, VCRs, and Set-Top boxes.

In addition, the Z86229 is ideally suited to monitor Line 21 video displayed in a PiP window for violence blocking, CCD, and other XDS data services. A block diagram of the Z86229 is illustrated in Figure 1.

Multistandard Sound Processor Family

Release Note: Revision bars indicate significant changes to the previous edition. The hardware and software description in this document is valid for the MSP 34x0G version B8 and following versions.

1. Introduction

The MSP 34x0G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure 1–1 shows a simplified functional block diagram of the MSP 34x0G.

This new generation of TV sound processing ICs now includes versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free.

Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 34x0G has optimum stereo performance without any adjustments.

All MSP 34xxG versions are pin compatible to the MSP 34xxD. Only minor modifications are necessary to adapt a MSP 34xxD controlling software to the MSP 34xxG. The MSP 34x0G further simplifies controlling software. Standard selection requires a single I^2C transmission only.

The MSP 34x0G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual; no I^2C interaction is necessary (Automatic Sound Selection).

The MSP 34x0G can handle very high FM deviations even in conjunction with NICAM processing. This is especially important for the introduction of NICAM in China.

The ICs are produced in submicron CMOS technology. The MSP 34x0G is available in the following packages: PLCC68 (not intended for new design), PSDIP64, PSDIP52, PQFP80, and PLQFP64.

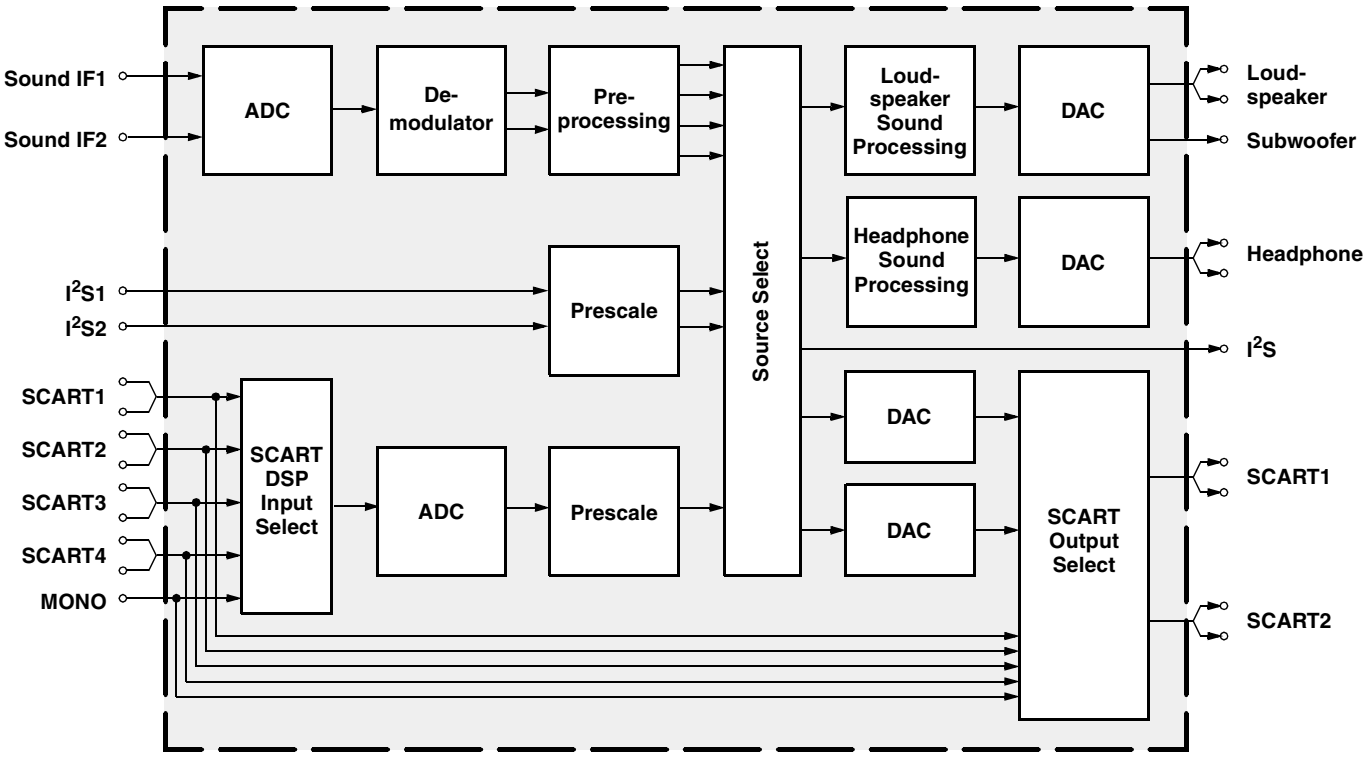


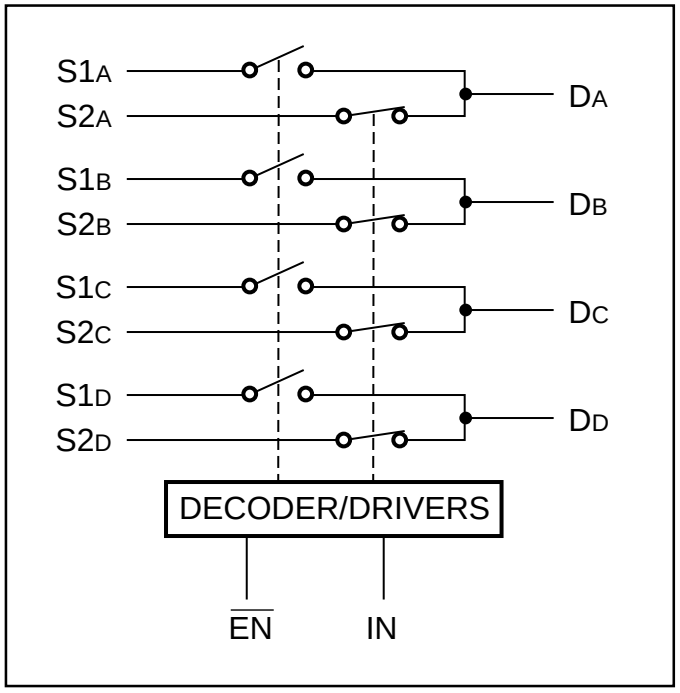
Fig. 1–1: Simplified functional block diagram of the MSP 34x0G

Low ON Resistance Wideband/Video Quad 2-Channel MUX/DEMUX

Product Features:

- High-performance, low-cost solution to switch between video sources
- Wide bandwidth: 200 MHz
- Low ON-resistance: 3Ω
- Low crosstalk at 10 MHz: –58 dB
- Ultra-low quiescent power (0.1 µA typical)
- Single supply operation: +5.0V
- Fast switching: 10 ns
- High-current output: 100 mA
- Packages available:
  - 16-pin 300-mil wide plastic SOIC (S)
  - 16-pin 150-mil wide plastic SOIC (W)
  - 16-pin 150-mil wide plastic QSOP (Q)

Functional Block Diagram



Truth Table

$\overline{EN}$	IN	ON Switch
0	0	$S1_A$, $S1_B$, $S1_C$, $S1_D$
0	1	$S2_A$, $S2_B$, $S2_C$, $S2_D$
1	X	Disabled

Product Description:

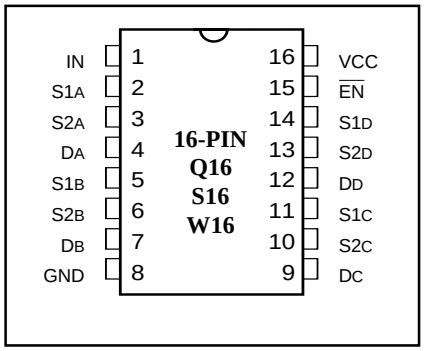
Pericom Semiconductor's PI5V series of mixed signal video circuits are produced in the Company's advanced CMOS low-power technology, achieving industry leading performance.

The PI5V330 is a true bidirectional Quad 2-channel multiplexer/demultiplexer that is recommended for both RGB and composite video switching applications. The VideoSwitch™ can be driven from a current output RAMDAC or voltage output composite video source.

Low ON-resistance and wide bandwidth make it ideal for video and other applications. Also this device has exceptionally high current capability which is far greater than most analog switches offered today. A single 5V supply is all that is required for operation.

The PI5V330 offers a high-performance, low-cost solution to switch between video sources. The application section describes the PI5V330 replacing the HC4053 multiplier and buffer/amplifier.

16-Pin Product Configuration



Product Pin Description

Pin Name	Description
$S1_A$, $S2_A$ $S1_B$, $S2_B$ $S1_C$, $S2_C$ $S1_D$, $S2_D$	Analog Video I/O
IN	Select Input
$\overline{EN}$	Enable
D_A, D_B, D_C, D_D	Analog Video I/O
GND	Ground
V_{CC}	Power

NIPPON PRECISION CIRCUITS INC.

SM5304AV

Video Buffer with Built-in Analog LPF

OVERVIEW

The SM5304AV is a 75Ω terminating resistance drive video buffer with built-in analog filter. The filter cutoff frequency, controlled by the resistance connected to RFC pin, can be set to match any system resolution. The output buffer can be selected 0dB, 6dB, and 12dB. The feedback point occurs after the external coupling capacitors, and the coupling capacitances can be reduced.

FEATURES

- 5V ± 10% supply voltage
- Adjustable cutoff frequency using external resistor
- 0dB, 6dB, 12dB selectable gain using logic signal
- ± 0.5dB output gain error
- Two systems (two load resistances) can be driven
- 0.7% output signal harmonic distortion
- Sag compensation circuit built-in
- Package: 8-pin VSOP (Pb free)

APPLICATIONS

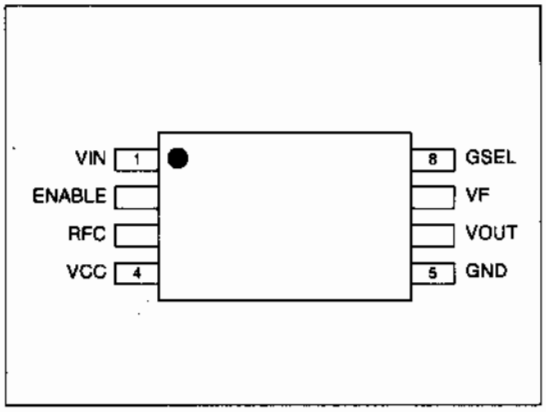
- DVD
- Digital still camera
- Digital VHS

ORDERING INFORMATION

Device	Package
SM5304AV	8-pin VSOP

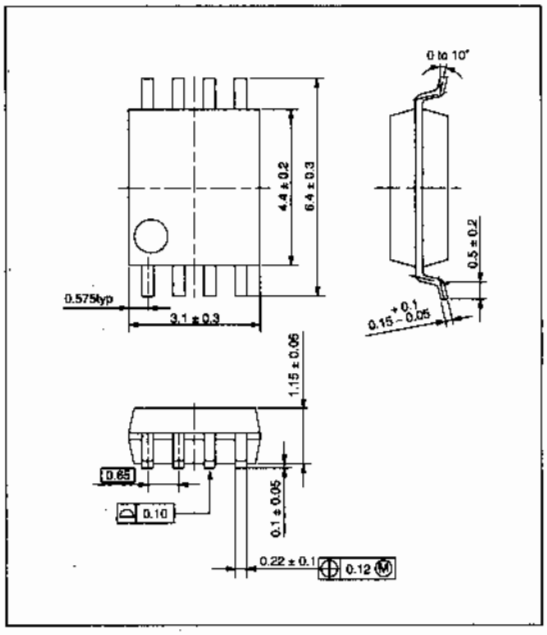
PINOUT

(Top view)

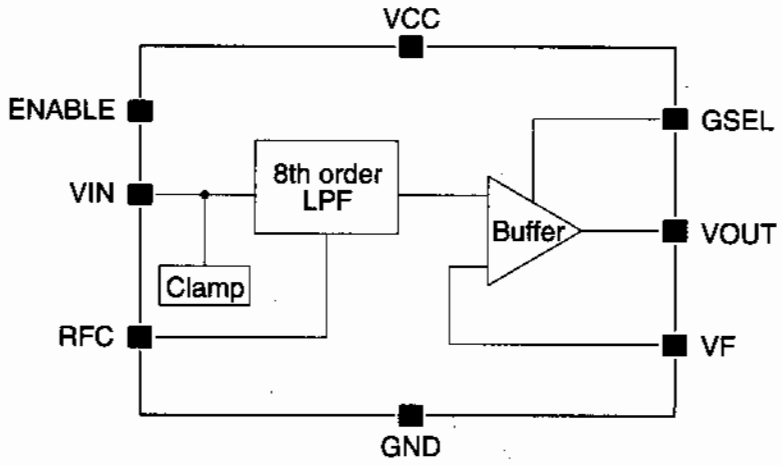


PACKAGE DIMENSIONS

(Unit: mm)
Weight: 0.04g



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O[1]	A/D[2]	Description
1	VIN	I	A	Input signal pin
2	ENABLE	I	D	Enable signal input pin (with pull-down resistor)
3	RFC	O	A	LPF cutoff frequency set pin
4	VCC	–	–	5V supply pin
5	GND	–	–	Ground pin
6	VOUT	O	A	Output signal pin
7	VF	I	A	Output signal feedback pin for sag compensation circuit
8	GSEL	I	D	Gain set signal input pin

1. I: input, O: output
2. A: analog, D: digital

2 x 12 W hi-fi audio power amplifiers with mute

TDA2616/TDA2616Q

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Excellent gain balance of both amplifiers
- Hi-fi in accordance with IEC 268 and DIN 45500
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION

The TDA2616 and TDA2616Q are dual power amplifiers. The TDA2616 is supplied in a 9-lead single-in-line (SIL9) plastic power package (SOT131), while the TDA2616Q is supplied in a 9-lead SIL-bent-to-DIL plastic power package (SOT157). They have been especially designed for mains fed applications, such as stereo radio and stereo TV.

QUICK REFERENCE DATA

Stereo application

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\pm V_P$	supply voltage range		7.5	–	21	V
P_O	output power	V_P = ±16 V; THD = 0.5%	–	12	–	W
G_v	internal voltage gain		–	30	–	dB
$\lvert G_v \rvert$	channel unbalance		–	0.2	–	dB
α	channel separation		–	70	–	dB
SVRR	supply voltage ripple rejection		–	60	–	dB
V_{no}	noise output voltage		–	70	–	μV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA2616	9	SIL	plastic	SOT131[1]
TDA2616Q	9	SIL-bent-to-DIL	plastic	SOT157[2]

Notes

1. SOT131-2; 1996 August 27.
2. SOT157-2; 1996 August 27.

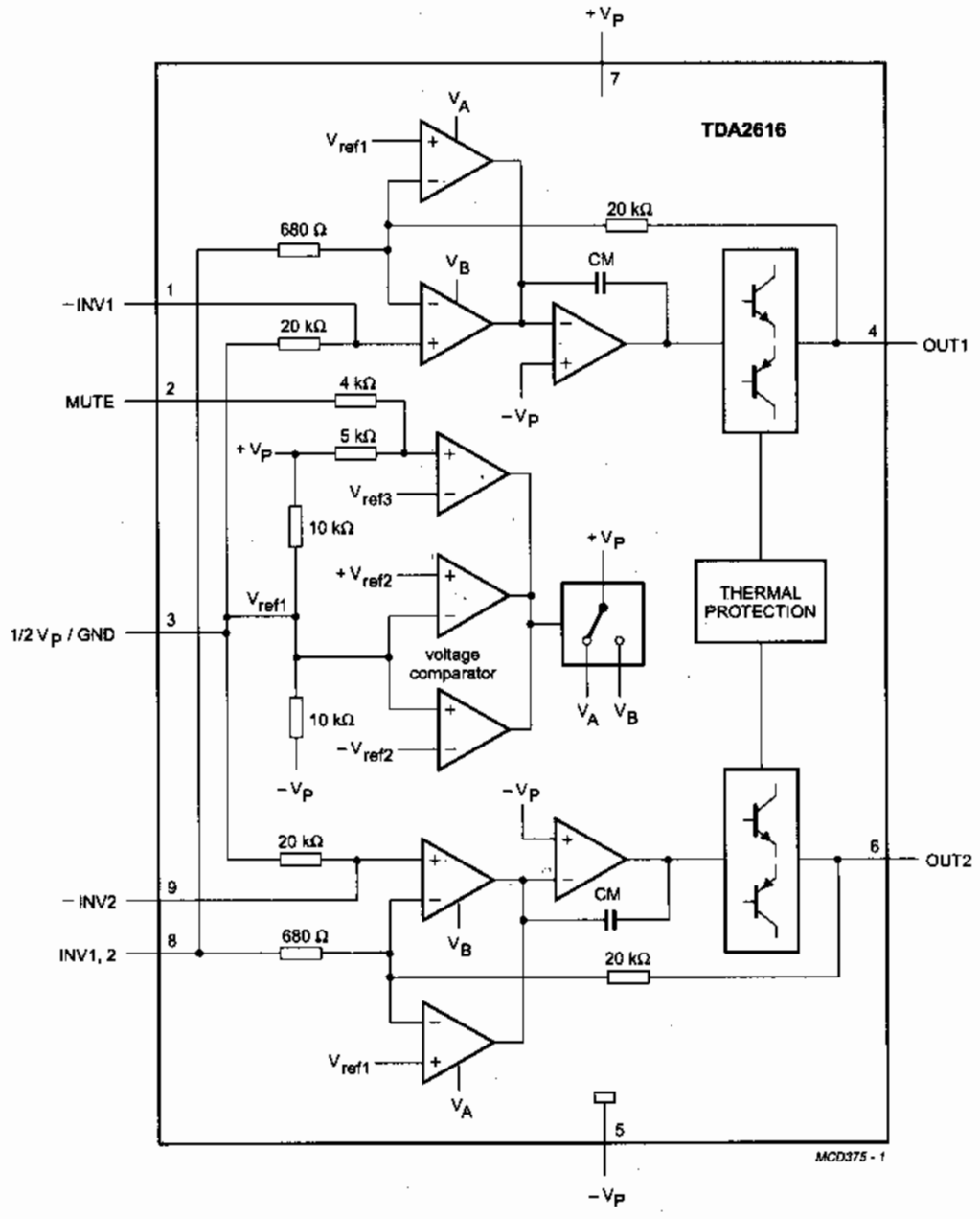


Fig.1 Block diagram.

1 FEATURES

- Support for 50 or 60 and 100 or 120 Hz and progressive scan display modes
- Complete 625 line teletext decoder in one chip reduces printed-circuit board area and cost
- Automatic detection of transmitted fastext links or service information (packet 8/30)
- On-Screen Display (OSD) for user interface menus using teletext and dedicated menu icons
- Video Programming System (VPS) decoding
- Wide Screen Signalling (WSS) decoding
- Pan-European, Cyrillic, Greek, Turkish, Arabic and Iranian character sets in each chip
- High-level command interface via I²C-bus gives easy control with a low software overhead
- High-level command interface is backward compatible to Stand-Alone Fastext And Remote Interface (SAFARI)
- 625 and 525 line display
- RGB interface to standard colour decoder ICs; current source
- Versatile 8-bit open-drain Input/Output (I/O) expander; 5 V tolerant
- Single 12 MHz crystal oscillator
- Single power supply: from 3.0 V to 3.6 V
- Operating temperature: −20 to +70 °C
- Automatic detection of transmitted pages to be selected by page up and page down
- 8 page fastext decoder
- Table Of Pages (TOP) decoder with Basic Top Table (BTT) and Additional Information Tables (AITs)
- 4 page user-defined list mode.

2 GENERAL DESCRIPTION

The SAA5360; SAA5361 is a single-chip multi page 625 line world system teletext decoder with a high-level command interface, and is SAFARI compatible.

The device is designed to minimize the overall system cost, due to the high-level command interface offering the benefit of a low software overhead in the TV microcontroller.

The SAA5360 incorporates the following functions:

- 10 page teletext decoder with OSD, fastext, TOP, default and list acquisition modes
- Automatic channel installation support.

The functionality of the SAA5361 is similar to the SAA5360, but offers the capability to store up to 250 additional pages of teletext in an external SRAM.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	all supply voltages	referenced to V_{SS}	3.0	3.3	3.6	V
I_{DDP}	periphery supply current	note 1	1	–	–	mA
I_{DDC}	core supply current	normal mode	–	15	18	mA
		idle mode	–	4.6	6	mA
I_{DDA}	analog supply current	normal mode	–	45	48	mA
		idle mode	–	0.87	1	mA
$f_{xtal(nom)}$	nominal crystal frequency	fundamental mode	–	12	–	MHz
T_{amb}	ambient temperature		−20	–	+70	°C
T_{stg}	storage temperature		−55	–	+125	°C

Note

1. Periphery supply current is dependent on external components and I/O voltage levels.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5360HL	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
SAA5361HL	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

5 BLOCK DIAGRAM

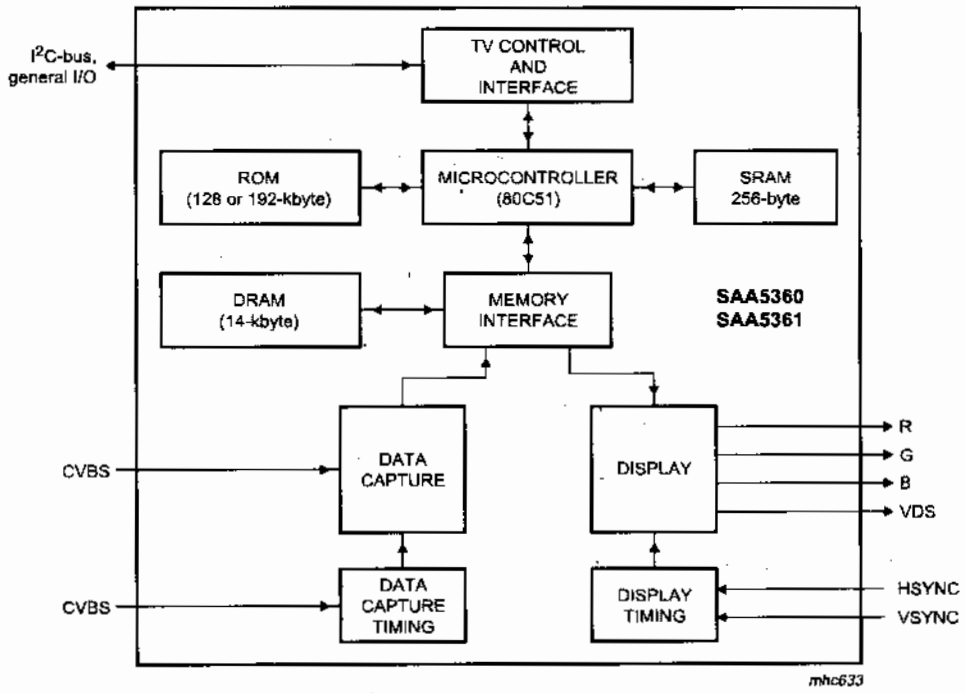


Fig.1 Block diagram.

Features

- **Low-Voltage and Standard-Voltage Operation**
  - **5.0 (V_{CC} = 4.5V to 5.5V)**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
  - **2.5 (V_{CC} = 2.5V to 5.5V)**
  - **1.8 (V_{CC} = 1.8V to 5.5V)**
- **Low-Power Devices (I_{SB} = 2 µA @ 5.5V) Available**
- **Internally Organized 4096 x 8, 8192 x 8**
- **2-Wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bidirectional Data Transfer Protocol**
- **100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Clock Rate**
- **Write Protect Pin for Hardware Data Protection**
- **32-Byte Page Write Mode (Partial Page Writes Allowed)**
- **Self-Timed Write Cycle (10 ms max)**
- **High Reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
  - **ESD Protection: >3,000V**
- **Automotive Grade and Extended Temperature Devices Available**
- **8-Pin JEDEC PDIP, 8-Pin JEDEC SOIC, 8-Pin EIAJ SOIC, and 8-pin TSSOP Packages**

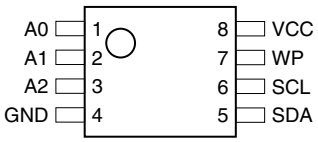
Description

The AT24C32/64 provides 32,768/65,536 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 4096/8192 words of 8 bits each. The device's cascadable feature allows up to 8 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C32/64 is available in space saving 8-pin JEDEC PDIP, 8-pin JEDEC SOIC, 8-pin EIAJ SOIC, and 8-pin TSSOP (AT24C64) packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

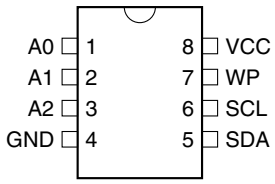
Pin Configurations

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

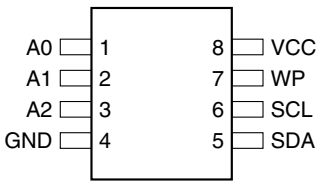
8-Pin TSSOP



8-Pin PDIP



8-Pin SOIC



2-Wire Serial EEPROM

32K (4096 x 8)

64K (8192 x 8)

AT24C32
AT24C64

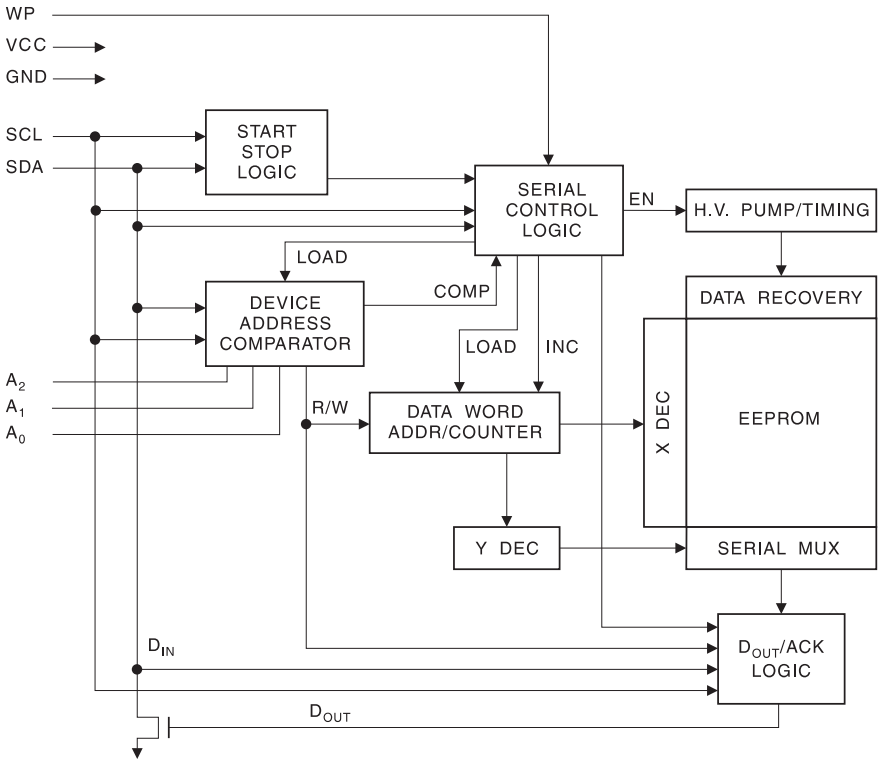
Rev. 0336G–04/01

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired or left not connected for hardware compatibility with AT24C16. When the pins are hardwired, as many as eight 32K/64K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). When the pins are not hardwired, the default A_2, A_1, and A_0 are zero.

WRITE PROTECT (WP): The write protect input, when tied to GND, allows normal write operations. When WP is tied high to V_{CC}, all write operations to the upper quandrant (8/16K bits) of memory are inhibited. If left unconnected, WP is internally pulled down to GND.

Memory Organization

AT24C32/64, 32K/64K SERIAL EEPROM: The 32K/64K is internally organized as 256 pages of 32 bytes each. Random word addressing requires a 12/13 bit data word address.

Features

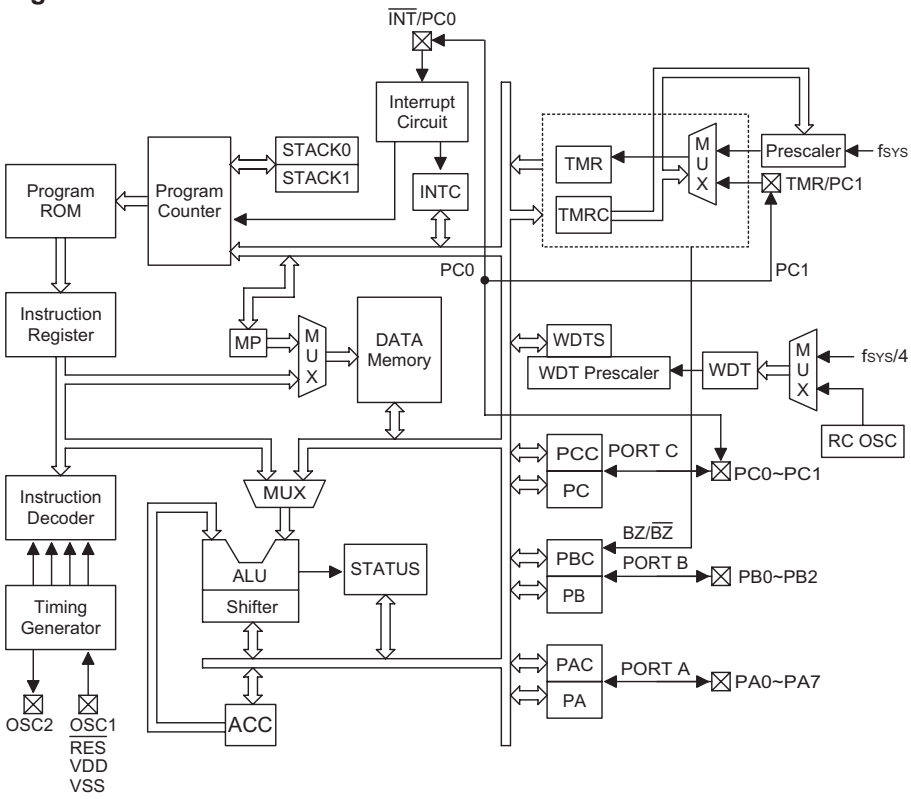
- Operating voltage:
  f_{SYS}=4MHz: 2.2V~5.5V
  f_{SYS}=8MHz: 3.3V~5.5V
- 13 bidirectional I/O lines
- An interrupt input shared with an I/O line
- 8-bit programmable timer/event counter with overflow interrupt and 8-stage prescaler
- On-chip crystal and RC oscillator
- Watchdog Timer
- 1024×14 program memory ROM
- 64×8 data memory RAM
- Buzzer driving pair and PFD supported
- HALT function and wake-up feature reduce power consumption
- Up to 0.5μs instruction cycle with 8MHz system clock at V_{DD}=5V
- All instructions in one or two machine cycles
- 14-bit table read instruction
- Two-level subroutine nesting
- Bit manipulation instruction
- 63 powerful instructions
- Low voltage reset function
- 16-pin SSOP package
  18-pin DIP/SOP package

General Description

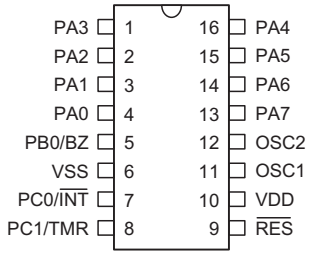
The HT48R06A-1/HT48C06 are 8-bit high performance, RISC architecture microcontroller devices specifically designed for cost-effective multiple I/O control product applications. The mask version HT48C06 is fully pin and functionally compatible with the OTP version HT48R06A-1 device.

The advantages of low power consumption, I/O flexibility, timer functions, oscillator options, HALT and wake-up functions, watchdog timer, buzzer driver, as well as low cost, enhance the versatility of these devices to suit a wide range of application possibilities such as industrial control, consumer products, subsystem controllers, etc.

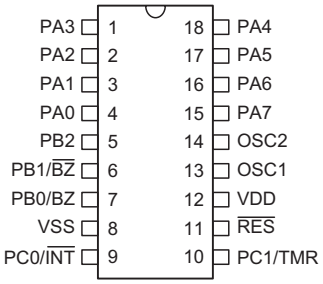
Block Diagram



Pin Assignment



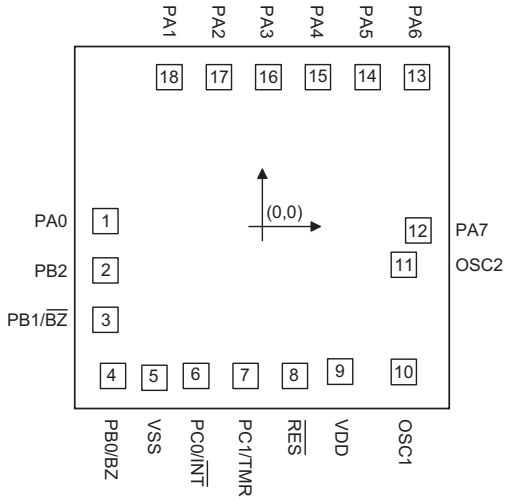
HT48R06A-1/HT48C06
– 16 SSOP-A



HT48R06A-1/HT48C06
– 18 DIP-A/SOP-A

Pad Assignment

HT48C06



* The IC substrate should be connected to VSS in the PCB layout artwork.

Pad Description

Pad Name	I/O	Options	Description
PA0~PA7	I/O	Pull-high* Wake-up	Bidirectional 8-bit input/output port. Each bit can be configured as wake-up input by options. Software instructions determine the CMOS output or Schmitt trigger input with a pull-high resistor (determined by pull-high options).
PB0/$\overline{BZ}$ PB1/$\overline{BZ}$ PB2	I/O	Pull-high* I/O or BZ/$\overline{BZ}$	Bidirectional 3-bit input/output port. Software instructions determine the CMOS output or Schmitt trigger input with a pull-high resistor (determined by pull-high options). The PB0 and PB1 are pin-shared with the BZ and $\overline{BZ}$, respectively. Once the PB0 and PB1 are selected as buzzer driving outputs, the output signals come from an internal PFD generator (shared with a timer/event counter).
VSS	—	—	Negative power supply, ground
PC0/$\overline{INT}$ PC1/TMR	I/O	Pull-high*	Bidirectional I/O lines. Software instructions determine the CMOS output or Schmitt trigger input with a pull-high resistor (determined by pull-high options). The external interrupt and timer input are pin-shared with the PC0 and PC1, respectively. The external interrupt input is activated on a high to low transition.
$\overline{RES}$	I	—	Schmitt trigger reset input. Active low
VDD	—	—	Positive power supply
OSC1 OSC2	I O	Crystal or RC	OSC1, OSC2 are connected to an RC network or Crystal (determined by options) for the internal system clock. In the case of RC operation, OSC2 is the output terminal for 1/4 system clock.

* All pull-high resistors are controlled by an option bit.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}–0.3V to V_{SS}+6.0V

Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature ..... –50°C to 125°C

Operating Temperature ..... –40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	f_{SYS}=4MHz	2.2	—	5.5	V
		—	f_{SYS}=8MHz	3.3	—	5.5	V
I_{DD1}	Operating Current (Crystal OSC)	3V	No load, f_{SYS}=4MHz	—	0.6	1.5	mA
		5V		—	2	4	mA
I_{DD2}	Operating Current (RC OSC)	3V	No load, f_{SYS}=4MHz	—	0.8	1.5	mA
		5V		—	2.5	4	mA
I_{DD3}	Operating Current (Crystal OSC)	5V	No load, f_{SYS}=8MHz	—	3	5	mA
I_{STB1}	Standby Current (WDT Enabled)	3V	No load, system HALT	—	—	5	μA
		5V		—	—	10	μA
I_{STB2}	Standby Current (WDT Disabled)	3V	No load, system HALT	—	—	1	μA
		5V		—	—	2	μA
V_{IL1}	Input Low Voltage for I/O Ports, TMR and $\overline{INT}$	—	—	0	—	$0.3V_{DD}$	V
V_{IH1}	Input High Voltage for I/O Ports, TMR and $\overline{INT}$	—	—	$0.7V_{DD}$	—	V_{DD}	V
V_{IL2}	Input Low Voltage ($\overline{RES}$)	—	—	0	—	$0.4V_{DD}$	V
V_{IH2}	Input High Voltage ($\overline{RES}$)	—	—	$0.9V_{DD}$	—	V_{DD}	V
V_{LVR}	Low Voltage Reset	—	LVR enabled	2.7	3.0	3.3	V
I_{OL}	I/O Port Sink Current	3V	V_{OL}=0.1V_{DD}	4	8	—	mA
		5V		10	20	—	mA
I_{OH}	I/O Port Source Current	3V	V_{OH}=0.9V_{DD}	–2	–4	—	mA
		5V		–5	–10	—	mA
R_{PH}	Pull-high Resistance	3V	—	40	60	80	kΩ
		5V	—	10	30	50	kΩ

MODEL : 50" HD D3.1 PDP

1,269cm (50 Inch) Wide Plasma Display Module

Quality Innovation Team

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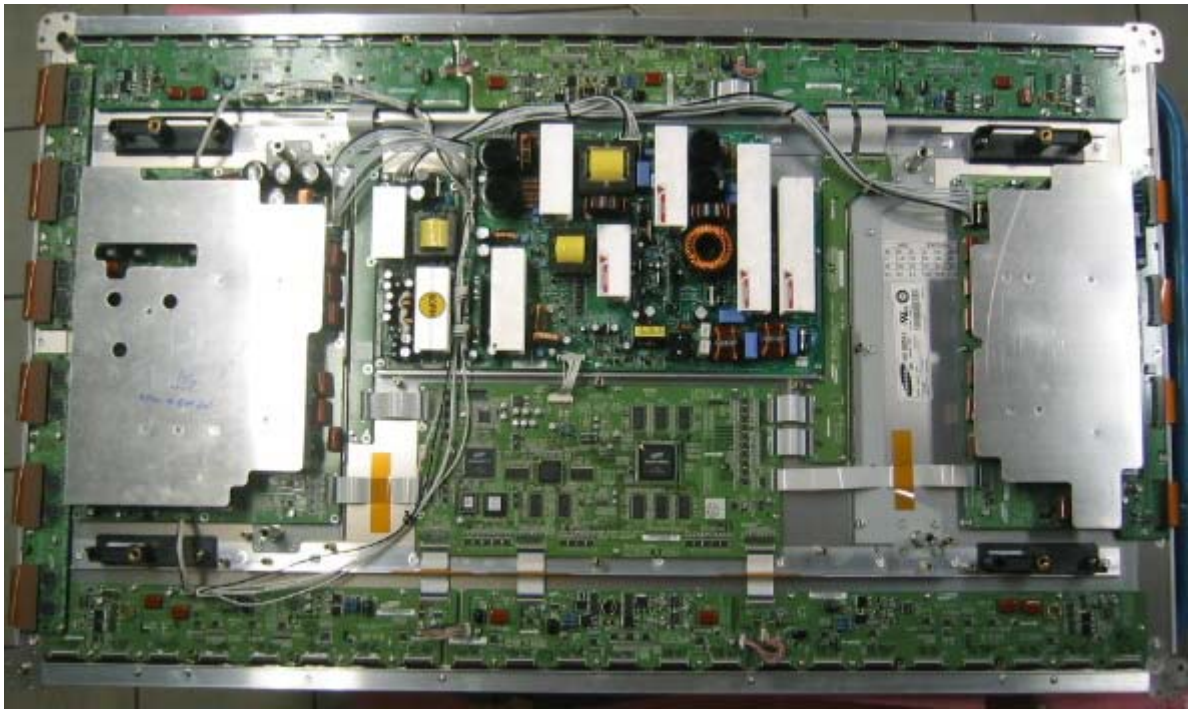
Formation and Specification of Module

1. Overview

1-1 Model Name of Plasma Display

MODEL : 50HD” D3.1 PDP (S50HW-XD03)

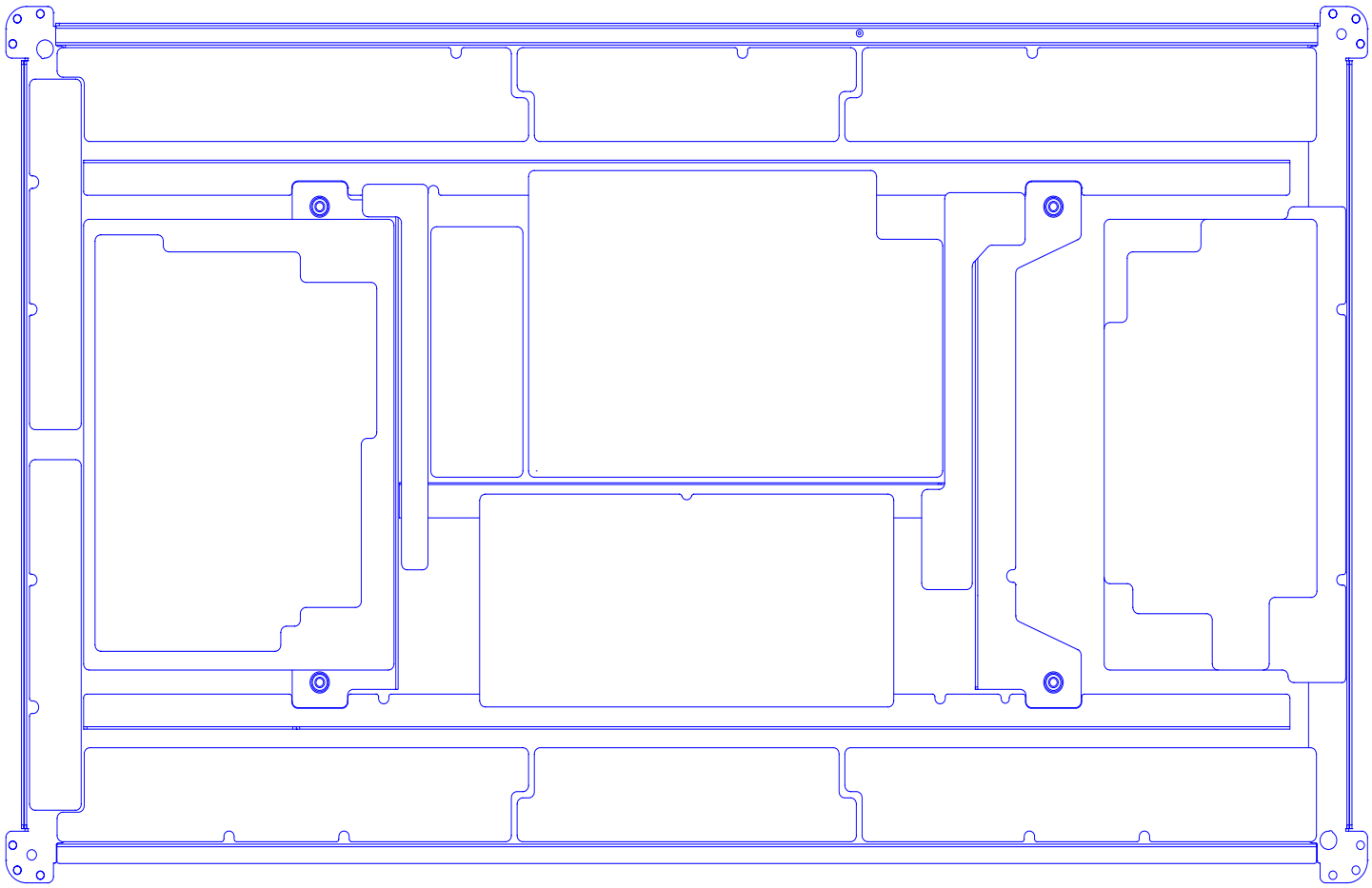
1-2 External View



【 M3 = X Board + Y Board + Logic Board + PSU + SUB PSU 】

Trouble Shooting

1-3 Points of Screw Mount



Blue Dot : SCREW 4X12

Red Dot : SCREW 3X10

1-4 Specifications

No	Item	Specification	
1	Pixel	Horizontal 1366 ×Vertical 768 pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	Horizontal 4,098 ×Vertical 768 cells	
3	Pixel Pitch	Horizontal 810μm ×Vertical 810μm	
4	Cell Pitch	R	Horizontal 270μm ×Vertical 810μm
		G	Horizontal 270μm ×Vertical 810μm
		B	Horizontal 270μm ×Vertical 810μm
5	Display size	Horizontal 1106.46㎜ ×Vertical 622.08㎜	
6	Screen size	Diagonal 50" Color Plasma Display Module	
7	Screen aspect	16 : 9	
8	Display color	16.77 million colors	
9	Viewing angle	Over 160° (Angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	1184(W) × 700 (H) × 60.1 (D) ㎜	
11	Weight	Module 1	About 18.0 kg
12	Packing weight	Module 1	140kg ± 5kg (including modules) / 5pcs/BOX
13	Packing size	L 760 * W 1465 * H 1106(mm) / 10pcs/BOX	
14	Broadcasting reception Vertical frequency and Video/Logic Interface		60Hz/ 50Hz, LVDS

2. Precaution

**** To prevent the risks of unit damage, electrical shock and radiation, take the following safety, service, and ESD precautions.**

2-1 Handling Precautions for Plasma Display

- PDP module use high voltage that is dangerous to human. Before operating PDP, always check the dust to prevent circuit short. Be careful touching the circuit device when power is on.
- PDP module is sensitive to dust and humidity. Therefore, assembling and disassembling must be done in no dust place.
- PDP module has a lot of electric devices. Service engineer must wear equipment(for example , earth ring) to prevent electric shock and working clothes to prevent electrostatic.
- PDP module use a fine pitch connector which is only working by exactly connecting with flat cable. Operator must pay attention to a complete connection when connector is reconnected after repairing.
- The capacitor's remaining voltage in the PDP module's circuit board temporarily remains after power is off. Operator must wait for discharging of remaining voltage during at least 1 minute.

2-2 Safety Precautions for Service (Handling, prevention of a electrical shock, measure against power outage, etc)

(Safety Precautions)

- Before replacing a board, discharge forcibly The remaining electricity from board.
- When connecting FFC and TCPs to the module, recheck that they are perfectly connected.
- To prevent electrical shock, be careful not to touch leads during circuit operatior
- To prevent the Logic circuit from being damaged due to wrong working, do not connect/disconnect signal cables during circuit operations.

- Do thoroughly adjustment of a voltage label and voltage-insulation.
- Before reinstalling the chassis and the chassis assembly, be sure to use all protective stuffs including a nonmetal controlling handle and the covering of partitioning type.
- Caution for design change : Do not install any additional devices to the module, and do not change the electrical circuit design.
- For example: Do not insert a subsidiary audio or video connector. If you insert It, It cause danger on safety. And, If you change the design or insert, Manufactor guarantee will be not effect. .
- If any parts of wire is overheats of damaged, replace it with a new specified one immediately, and identify the cause of the problem and remove the possible dangerous factors.
- Examine carefully the cable status if it is twisted or damaged or displaced. Do not change the space between parts and circuit board. Check the cord of AC power preparing damage.
- Product Safety Mark : Some of electric or implement material have special characteristics invisible that was related on safety. In case of the parts are changed with new one, even though the Voltage and Watt is higher than before, the Safety and Protection function will be lost.
- The AC power always should be turned off, before next repair..
- Check assembly condition of screw, parts and wire arrangement after repairing. Check whether the material around the parts get damaged.

(Precaution when repairing ESD)

- There is ESD which is easily damaged by electrostatics.(for example Integrated circuit, FET) Electrostatic damage rate of product will be reduced by the following technics
- Before handling semiconductor parts/assembly, must remove positive electric by ground connection, or must wear the antistatic wrist-belt and ring. (It must be operated after removing dust on it – It comes under precaution of electric shock.)

- After removing ESD assembly, put on it with aluminum stuff on the conductive surface to prevent charging.

- Do not use chemical stuff using Freon. It generates positive electric that can damage ESD.

- Must use a soldering device for ground-tip when soldering or de-soldering ESD.

- Must use anti-static solder removal device. Most removal device do not have antistatic which can charge a enough positive electric enough damaging ESD.

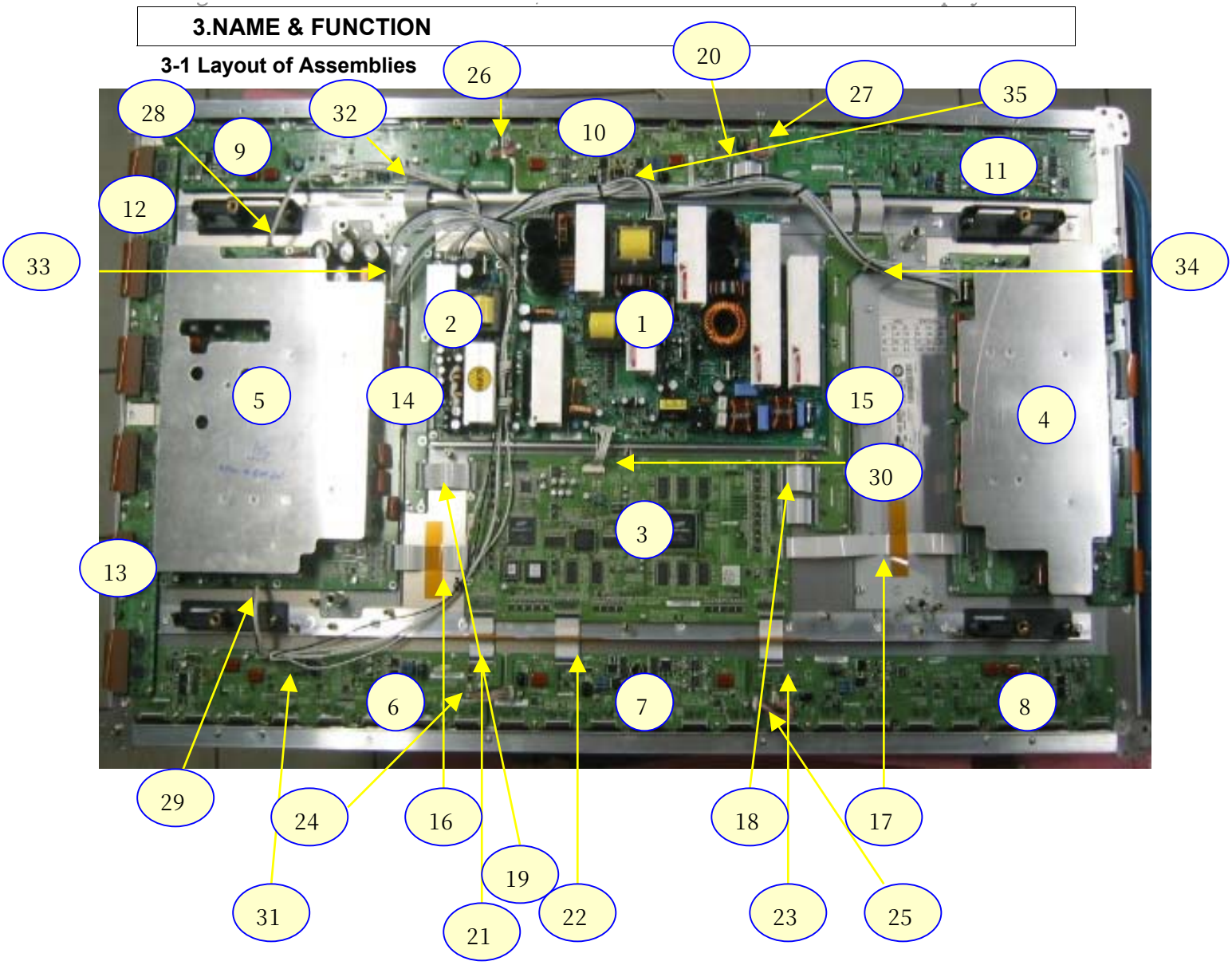
- Before removeing the protective material from the lead of a new ESD, bring the protective material into contact with the chassis or assembly that the ESD is to be installed on.

- When handing an unpacked ESD for replacement, do not move around too much. Moving (legs on the carpet, for example) generates enough electrostatic to damage the ESD.

- Do not take a new ESD from the protective case until the ESD is ready to be installed. Most ESD have a lead, which is easily short-circuited by conductive materials (such as conductive foam and aluminum)

3.NAME & FUNCTION

3-1 Layout of Assemblies



No.	Code No.	Location	Name
1	LJ44-00065A	Main PUS	ASSY PCB PSU
2	LJ44-00099A	SUB-PSU	ASSY PCB SUB-PSU
3	LJ92-00949C	LOGIC-MAIN Board	ASSY PCB LOGIC MAIN
4	LJ92-00852A	X-MAIN Driving Board	ASSY PCB X MAIN
5	LJ92-00853A	Y-MAIN Driving Board	ASSY PCBY MAIN
6	LJ92-00917A	LOGIC E BUFFER Board	ASSY PCB BUFFER
7	LJ92-00918A	LOGIC F BUFFER Board	ASSY PCB BUFFER
8	LJ92-00919A	LOGIC G BUFFER Board	ASSY PCB BUFFER
9	LJ92-00920A	LOGIC H BUFFER Board	ASSY PCB BUFFER
10	LJ92-00921A	LOGIC I BUFFER Board	ASSY PCB BUFFER
11	LJ92-00922A	LOGIC J BUFFER Board	ASSY PCB BUFFER
12	LJ92-00880A	Y-BUFFER (UPPER) Board	ASSY PCB BUFFER
13	LJ92-00881A	Y-BUFFER (DOWN) Board	ASSY PCB BUFFER
14	LJ92-00959A	SUB-R	ASSY PCB BUFFER
15	LJ92-00923A	SUB-L	ASSY PCB BUFFER
16	3809-001526	LOGIC + Y-MAIN	FFC CABLE-FLAT
17	3809-001516	LOGIC + X-MAIN	FFC CABLE-FLAT
18	3809-001414	SUB R + LOGIC	FFC CABLE-FLAT
19	3809-001414	SUB L + LOGIC	FFC CABLE-FLAT
20	3809-001414	LOGIC BUF(I) + LOGIC BUF(J) (UP)	FFC CABLE-FLAT
21	3809-001415	LOGIC + LOGIC BUF(E)(Down)	FFC CABLE-FLAT
22	3809-001415	LOGIC + LOGIC BUF(F)(Down)	FFC CABLE-FLAT
23	3809-001415	LOGIC + LOGIC BUF(G)(Down)	FFC CABLE-FLAT
24	LJ39-00121A	LOGIC BUF(E) + LOGIC BUF(F)	LEAD CONNECTOR
25	LJ39-00121A	LOGIC BUF(F) + LOGIC BUF(G)	LEAD CONNECTOR
26	LJ39-00121A	LOGIC BUF(H) + LOGIC BUF(I)	LEAD CONNECTOR
27	LJ39-00121A	LOGIC BUF(I) + LOGIC BUF(J)	LEAD CONNECTOR
28	LJ39-00122A	Y-MAIN + LOGIC BUF(H)	LEAD CONNECTOR
29	LJ39-00122A	Y-MAIN + LOGIC BUF(E)	LEAD CONNECTOR
30	LJ39-00113A	PSU + LOGIC MAIN	LEAD CONNECTOR
31	LJ39-00118A	PSU + LOGIC BUF(E)	LEAD CONNECTOR
32	LJ39-00177A	PSU + LOGIC BUF(H)	LEAD CONNECTOR
33	LJ39-00175A	PSU + Y-MAIN	LEAD CONNECTOR
34	LJ39-00173A	PSU + X-MAIN	LEAD CONNECTOR
35	LJ39-00178A	PSU + SUB PSU	LEAD CONNECTOR

1. L-Main	2.X-Main
3. Y-Main	**3. E-Buffer**
4, F-Buffer	**5. G-Buffer**
7. H-Buffer	**8. I-Buffer**

9. J-Buffer	10. Y-Buffer (lower)
11. Y-Buffer (Down)	**12. Sub-R**
13. Sub-L	

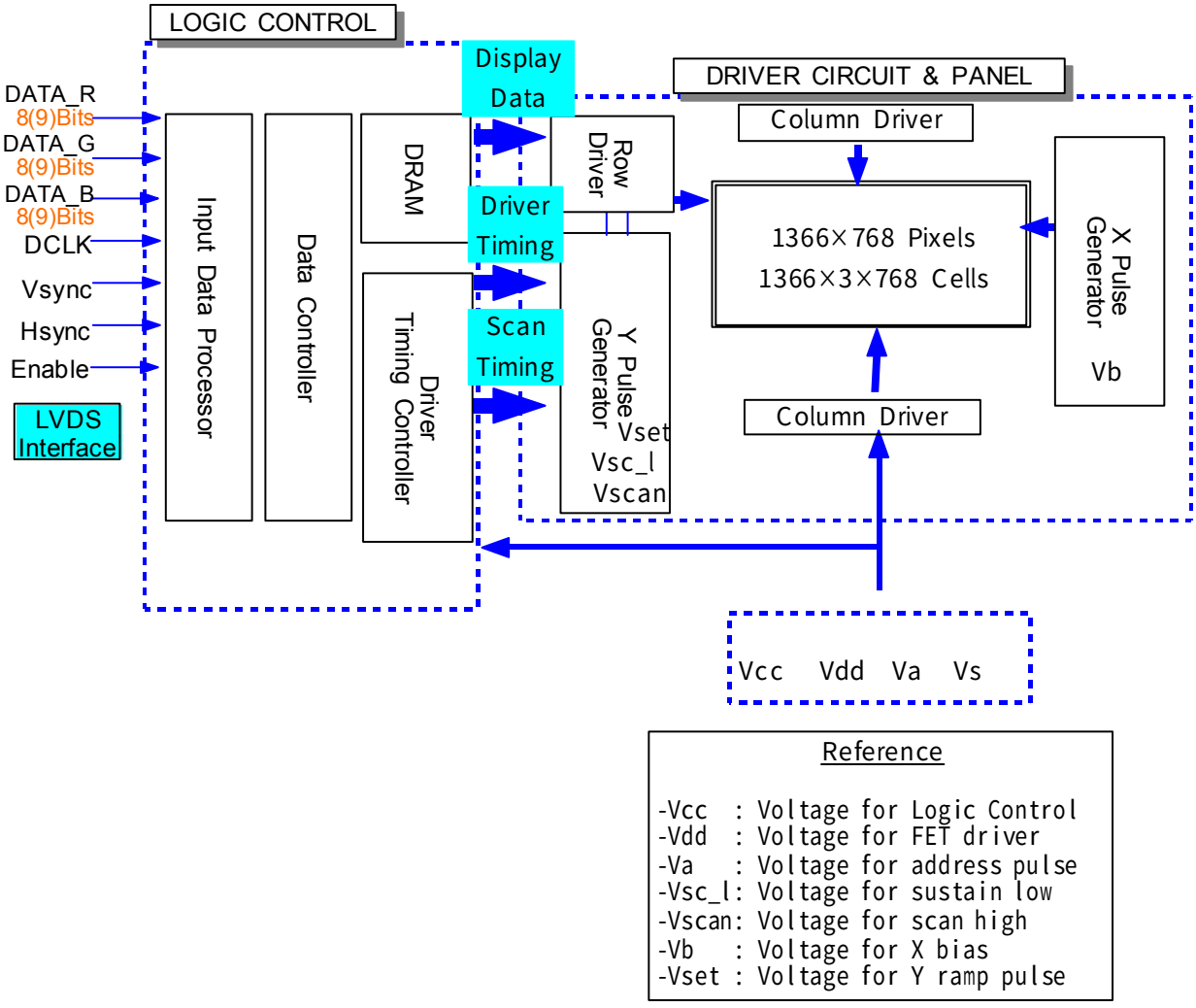
3-2 BLOCK DIAGRAM

3-2-1 BLOCK DIAGRAM FOR DRIVE CIRCUIT OPERATION

To be Updated

3-2-2 Block Diagram for Logic circuit

Block Diagram



3-3 Main function of Each Assembly

■ X-main board : The X-main board generate a drive signal by switching the FET in synchronization with logic main board timing and supplies the X electrode of the panel with the drive signal through the connector.

1) Maintain voltage waveforms (including ERC)
2) Generate X rising ramp signal
3) Maintain Ve bias between Scan intervals

■.Y-main board : The Y-main board generate a drive signal by switching the FET in synchronization with the logic Main Board timing and sequentially supplies the Y electrode of the panel with the drive signal through the scan driver IC on the Y-buffer board. This board connected to the panel's Y terminal has the following main functions.

1) Maintain voltage waveforms (including ERC)

2) Generate Y-rising Falling Ramp

3) Maintain V scan bias

■ Logic main board : The logic main board generates and outputs the address drive output signal and the X ,Y drive signal by processing the video signals. This Board buffers the address dirve output signal and feeds it to the address drive IC (COF module)

(video signal- X Y drive signal generation , frame memory circuit / address data rearrangement)

■.Logic buffer(E,F) : The logic buffer transmits data signal and control signal.

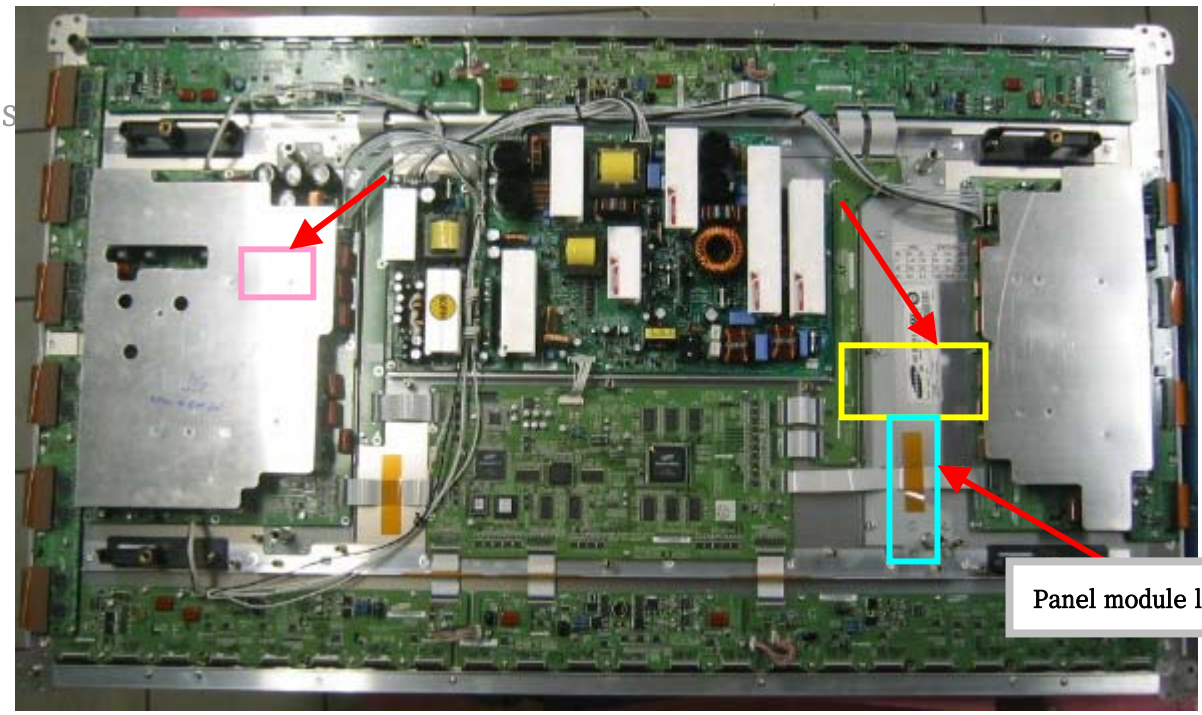
■.Y-buffer board (Upper, Lower) : The Y-buffer board consisting of the upper and lower boards supplies the Y-terminal with scan waveforms. The board comprises 8 scan driver IC's (ST microelectronics STV 7617 : 64 or 65 output pins) , but 4 ICs for the SD class

■.AC Noise Filter : The AC Noise filter has function for removing noise(low Frequency) and blocking surge. It effects Safety standards(EMC,EMI)

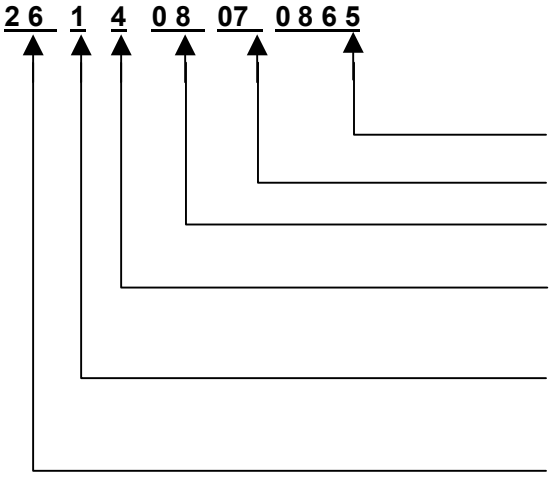
■.TCP(Tape Carrier Package) : The TCP applies Va pulse to the address electrode and constitutes address discharge by the potential difference between the Va pulse and the pulse applied to the Y electrode. The TCP comprise 4 data driver Ics(STV7610A :96 pins output pins) 7 TCPs are required for signal scan

.

3-4 PRODUCT/ SERIAL LABEL LOCATION



3-4-1 Serial No.



Serial No : 0001~9999
Date : 01~31
Month : 01~12
Year : 00(2000) ~99(2099)
Line No : 1 ~ 9 (0:Pilot Line)
Type : 02~48 **(ex.50HDv3:26)** (Step of even)

4. OPERATION CHECKING AFTER RECTIFICATION

4-1 Flow chart

* A/S Check Point *

1.Checking the voltage for each assembly

↓

2. Judging the Logic board working or not [Vsync, 3.3V, 5V]

↓

3. Adjusting the output signal through test points

↓

4. Checking the panel's crack

4-1-1 No voltage output

Check CN8001/2pin
Connect [220Vac]
LED 8004;Green

Ac Input

NG → Reconnect it

OK

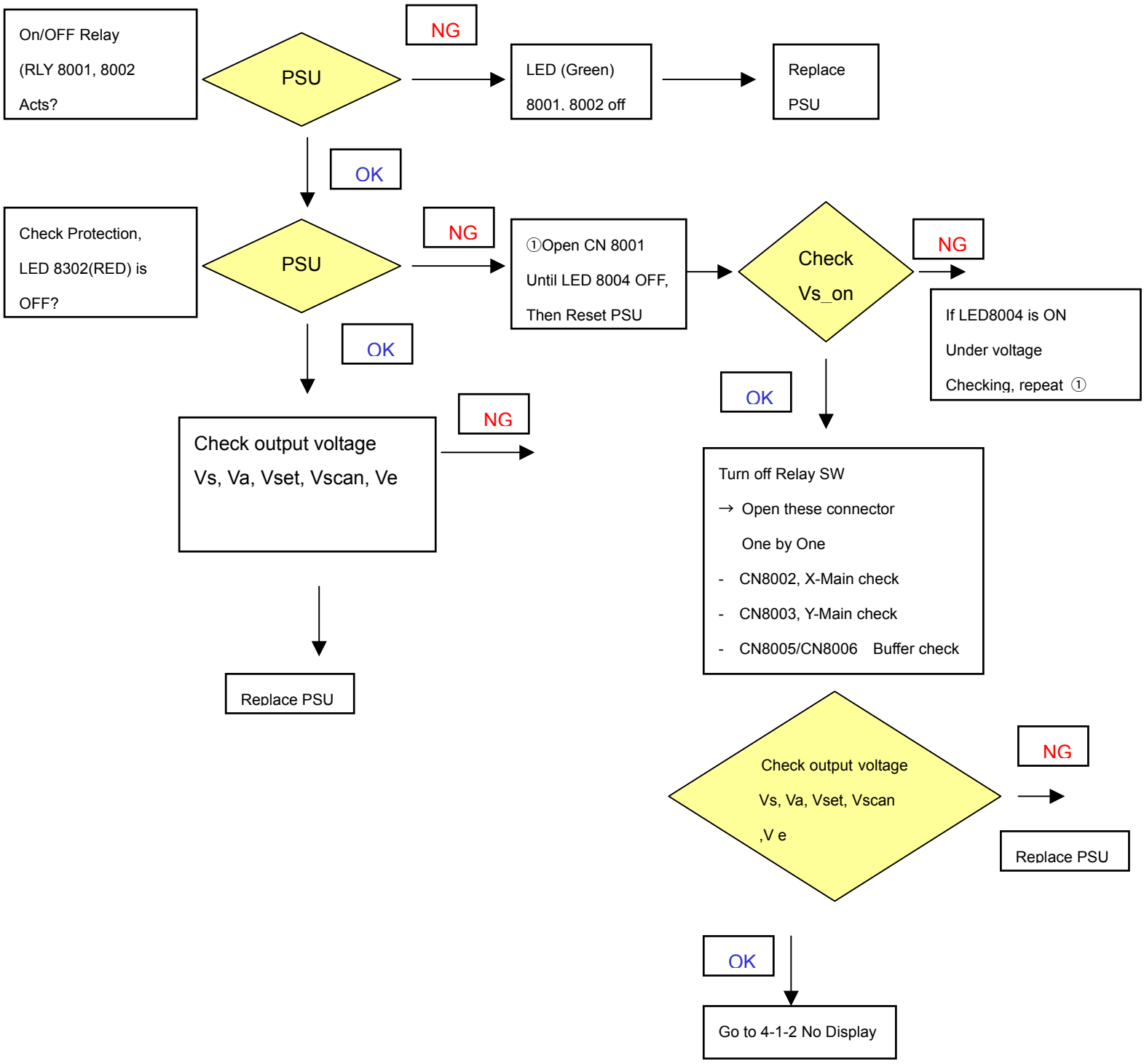
Check
LED 8001,8002
Green

①PSU

NG →

PSU Voltage check

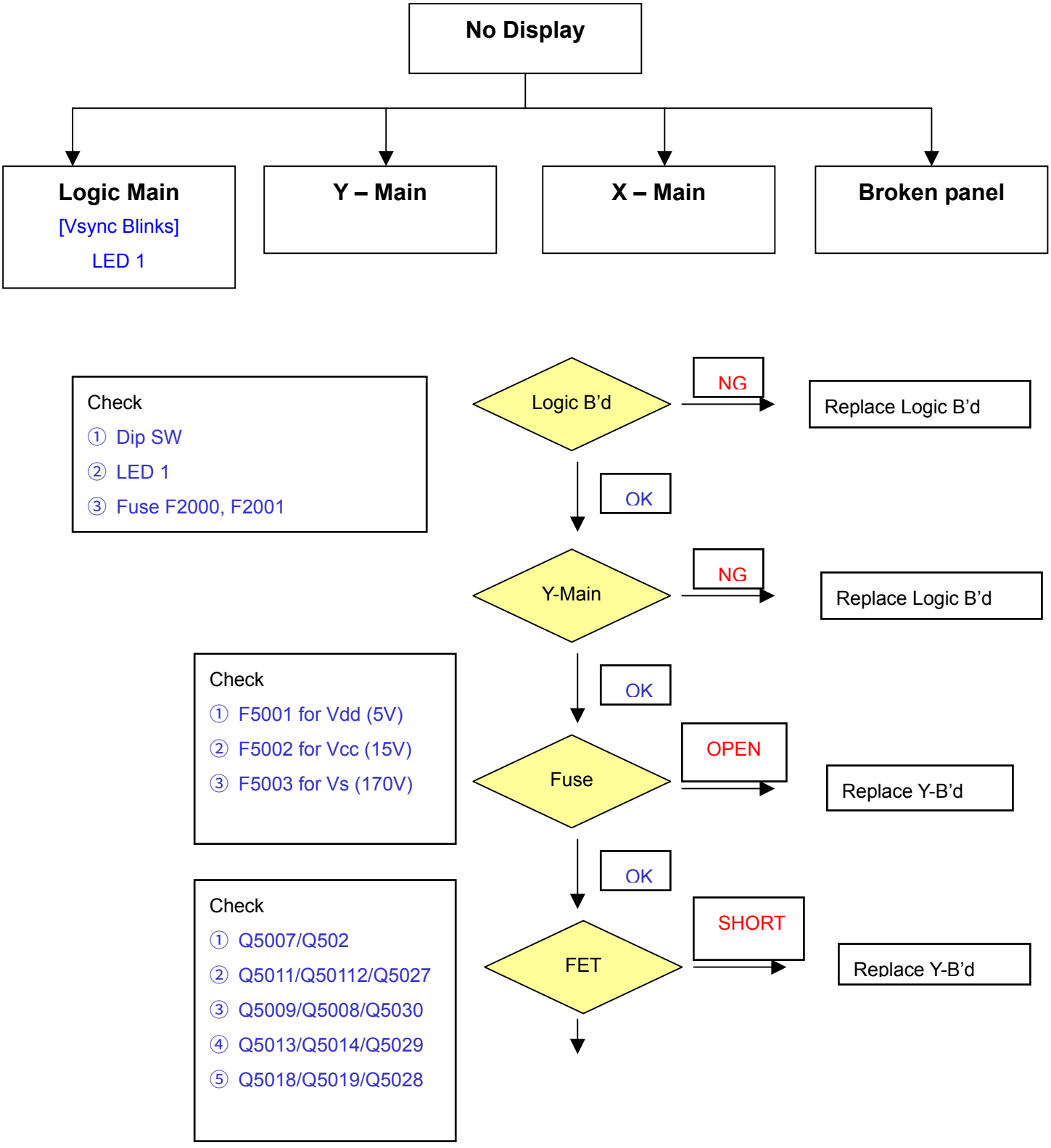
D5V; 5V Check
Vs ; 170V Check
Va ; 72V Check
Vset; 180V Check
Vscan; -90V Check
Vb; 155V Check
Vcc; 15V Check
Vcan_h; 25V Check
D3V3; 3.3V Check
9Vstandby;9V Check
Fuse 8001/8002/8003

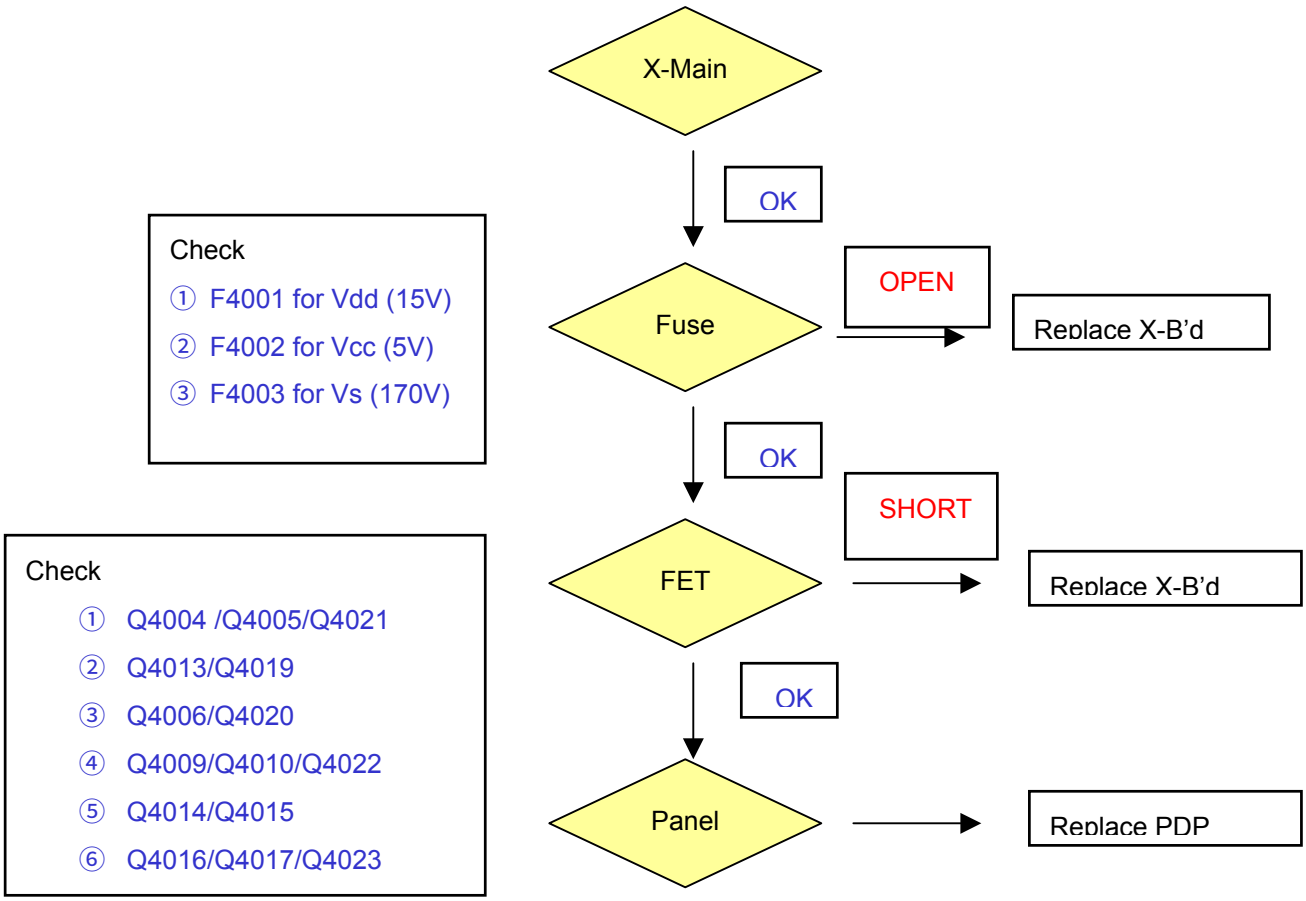

On/OFF Relay
(RLY 8001, 8002
Acts?
PSU
NG
LED (Green)
8001, 8002 off
Replace
PSU
OK
Check Protection,
LED 8302(RED) is
OFF?
PSU
NG
①Open CN 8001
Until LED 8004 OFF,
Then Reset PSU
Check
Vs_on
NG
If LED8004 is ON
Under voltage
Checking, repeat ①
OK
OK
Check output voltage
Vs, Va, Vset, Vscan, Ve
NG
Turn off Relay SW
→ Open these connector
One by One
- CN8002, X-Main check
- CN8003, Y-Main check
- CN8005/CN8006 Buffer check
Replace PSU
Check output voltage
Vs, Va, Vset, Vscan
,V e
NG
Replace PSU
OK
Go to 4-1-2 No Display

4-1-2 NO display (operating Voltage but an image doesn't exist on Screen)

⇒ No Display is related with Y-MAIN, X-MAIN, Logic Main and so on.

This page shows you how to check the boards, and the following pages show you how to find the defective board.

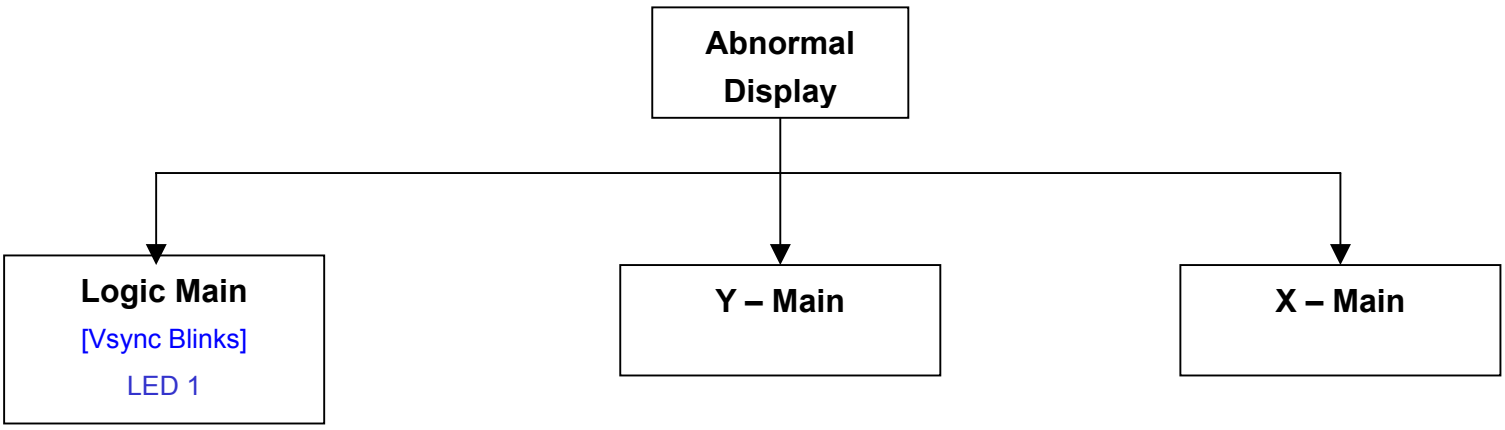


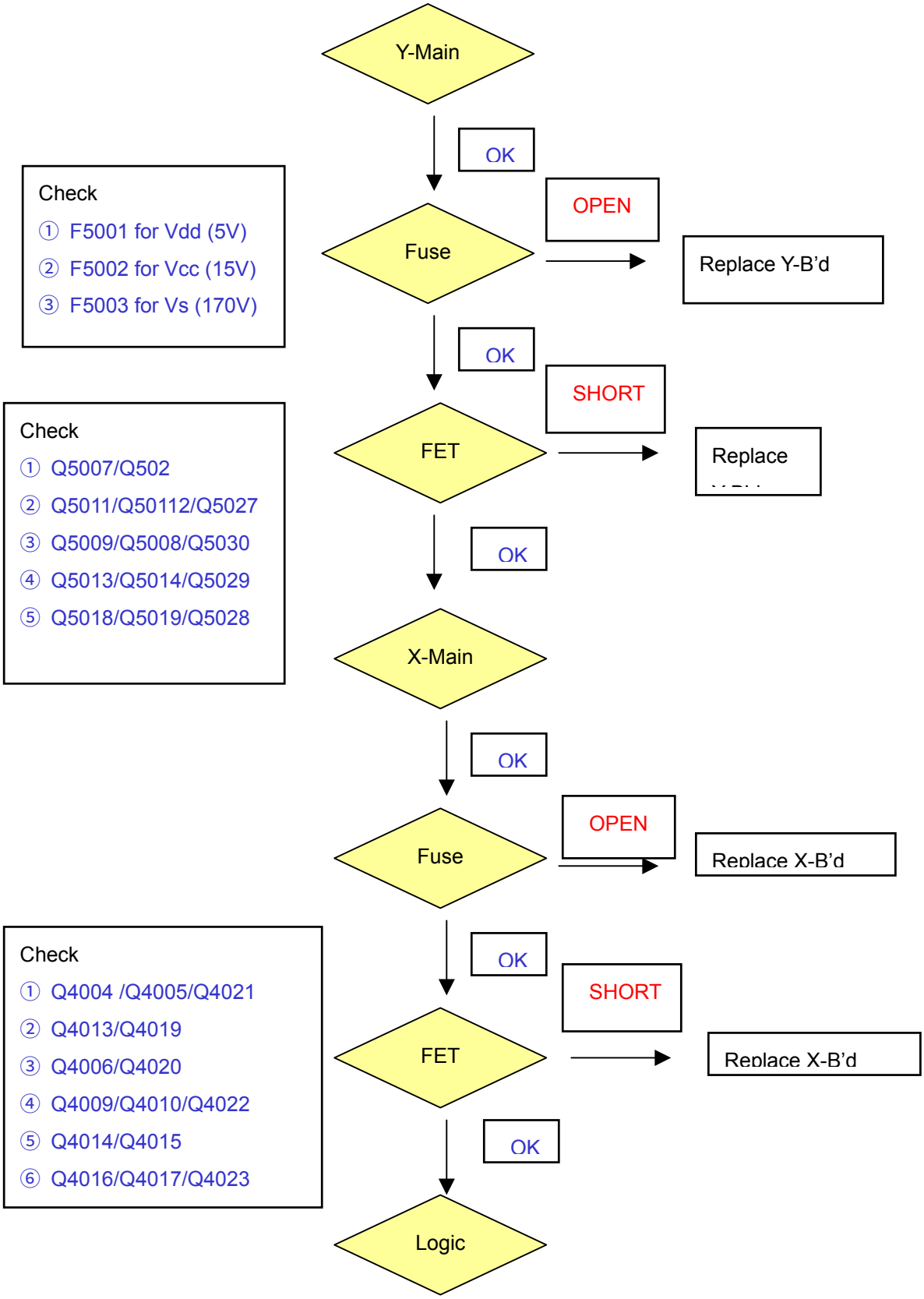


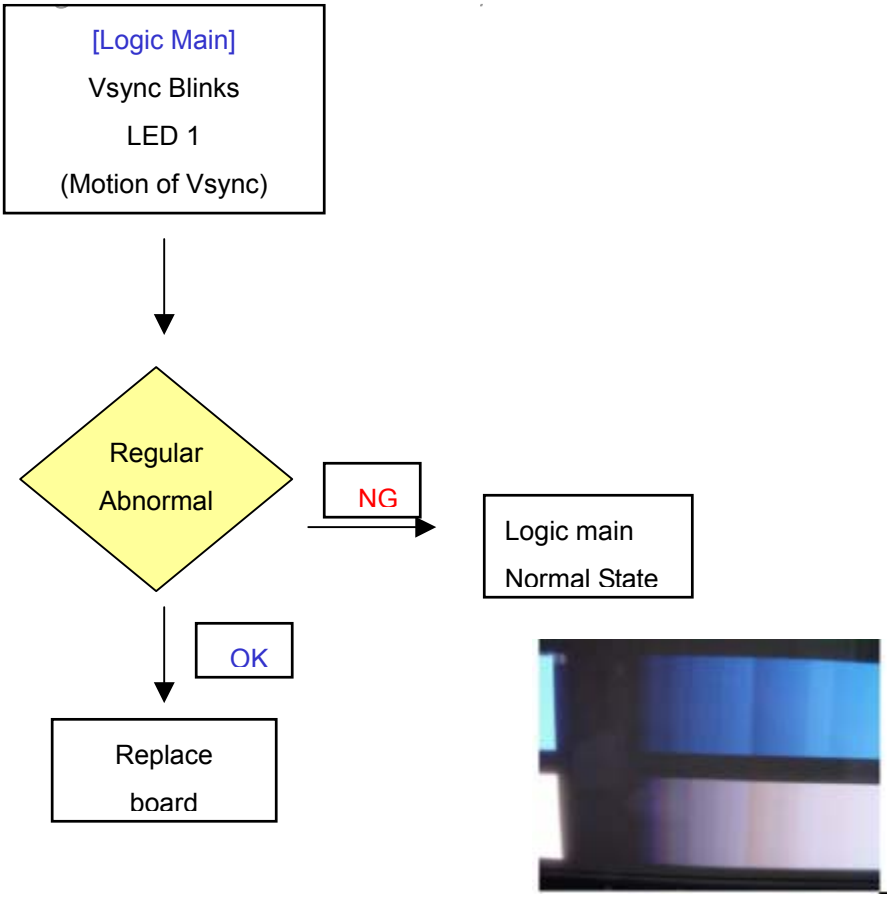
4-1-3 Abnormal Display (Abnormal Image is on Screen. (except abnormality in Sustain or Address)

⇒ Abnormal Display is related with Y-MAIN, X-MAIN, Logic Main and so on.

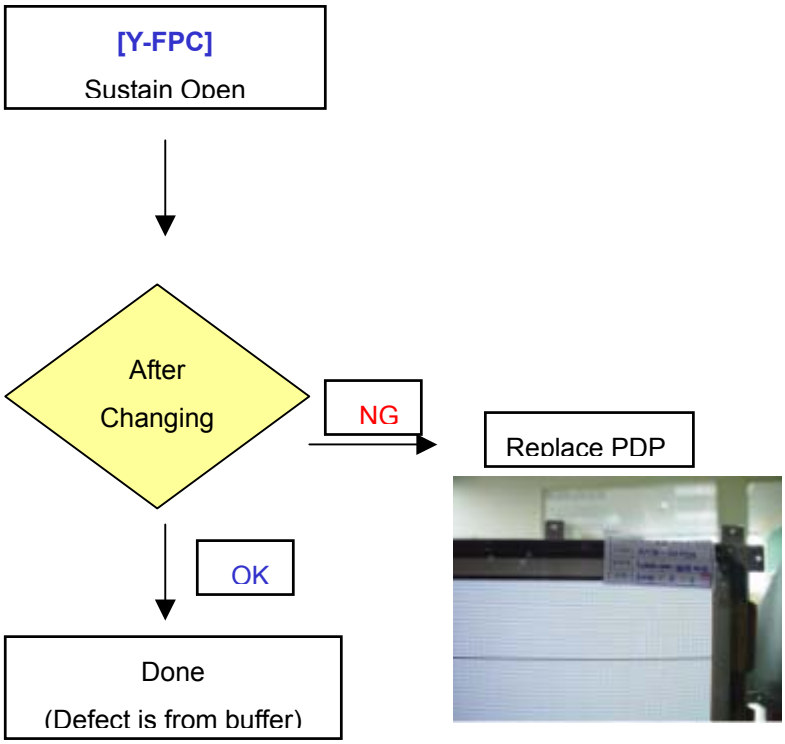
This page shows you how to check the boards, and the following pages show you how to find the defective board.



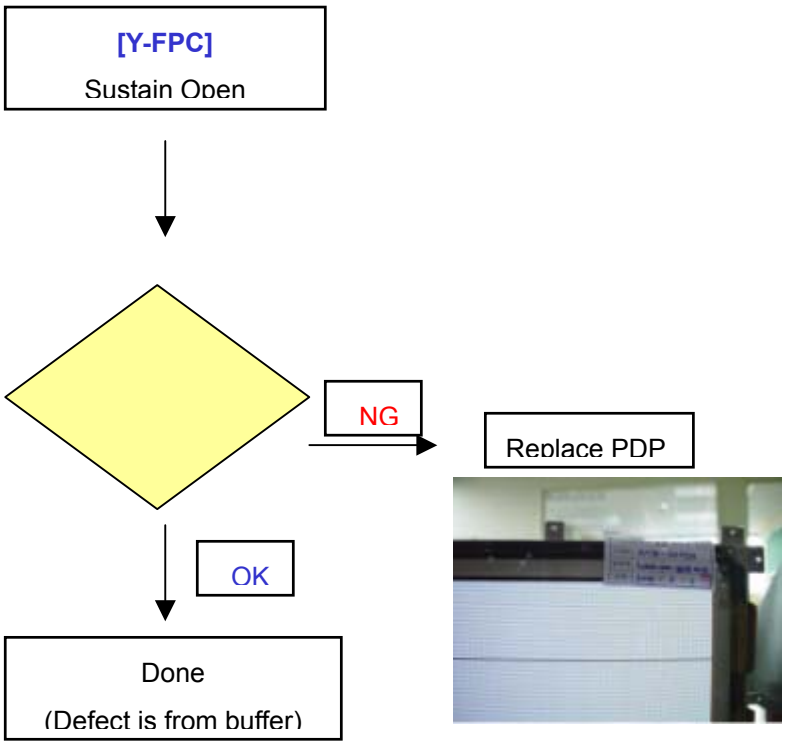

Y-Main
OK
Check
① F5001 for Vdd (5V)
② F5002 for Vcc (15V)
③ F5003 for Vs (170V)
Fuse
OPEN
Replace Y-B'd
OK
SHORT
Check
① Q5007/Q502
② Q5011/Q50112/Q5027
③ Q5009/Q5008/Q5030
④ Q5013/Q5014/Q5029
⑤ Q5018/Q5019/Q5028
FET
Replace
OK
X-Main
OK
Fuse
OPEN
Replace X-B'd
OK
SHORT
Check
① Q4004 /Q4005/Q4021
② Q4013/Q4019
③ Q4006/Q4020
④ Q4009/Q4010/Q4022
⑤ Q4014/Q4015
⑥ Q4016/Q4017/Q4023
FET
Replace X-B'd
OK
Logic



4-1-4 Sustain Open (some horizontal lines don't exist on screen)

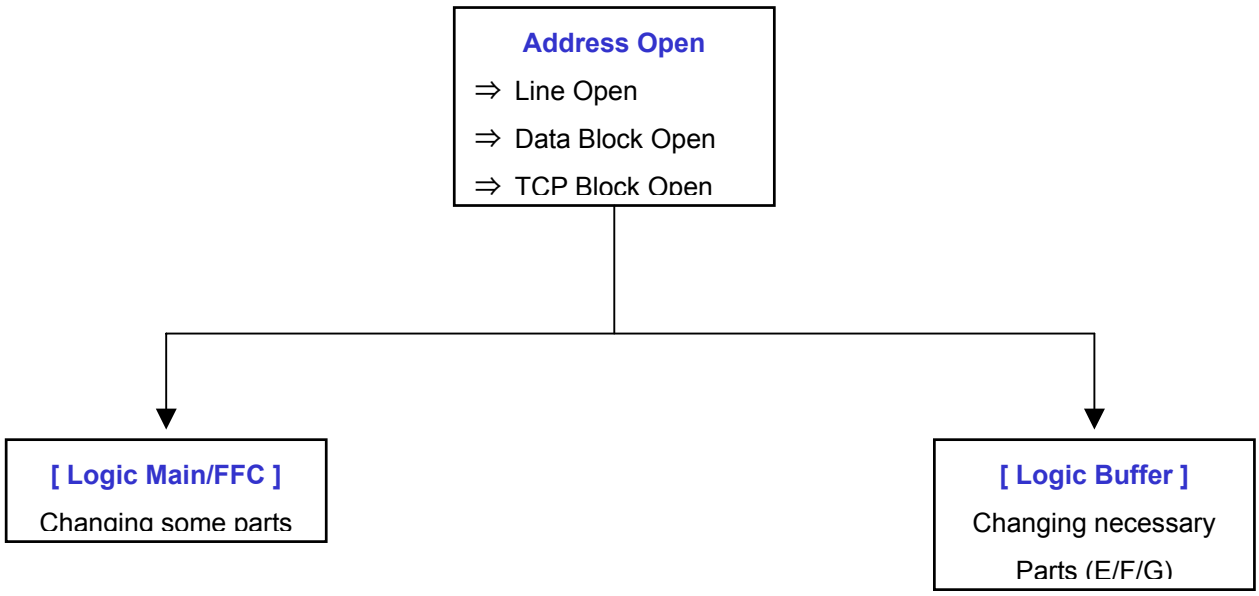


4-1-5 Sustain Short (some horizontal lines appear to be linked on Video)



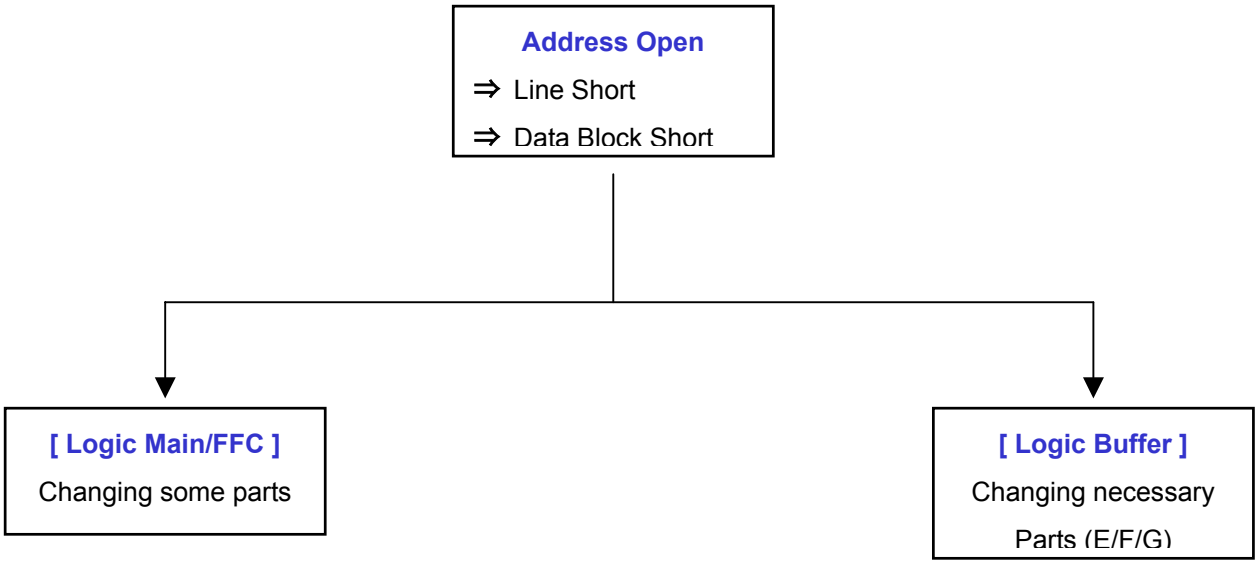
4-1-6 Address Open (some vertical lines don't exist on screen)

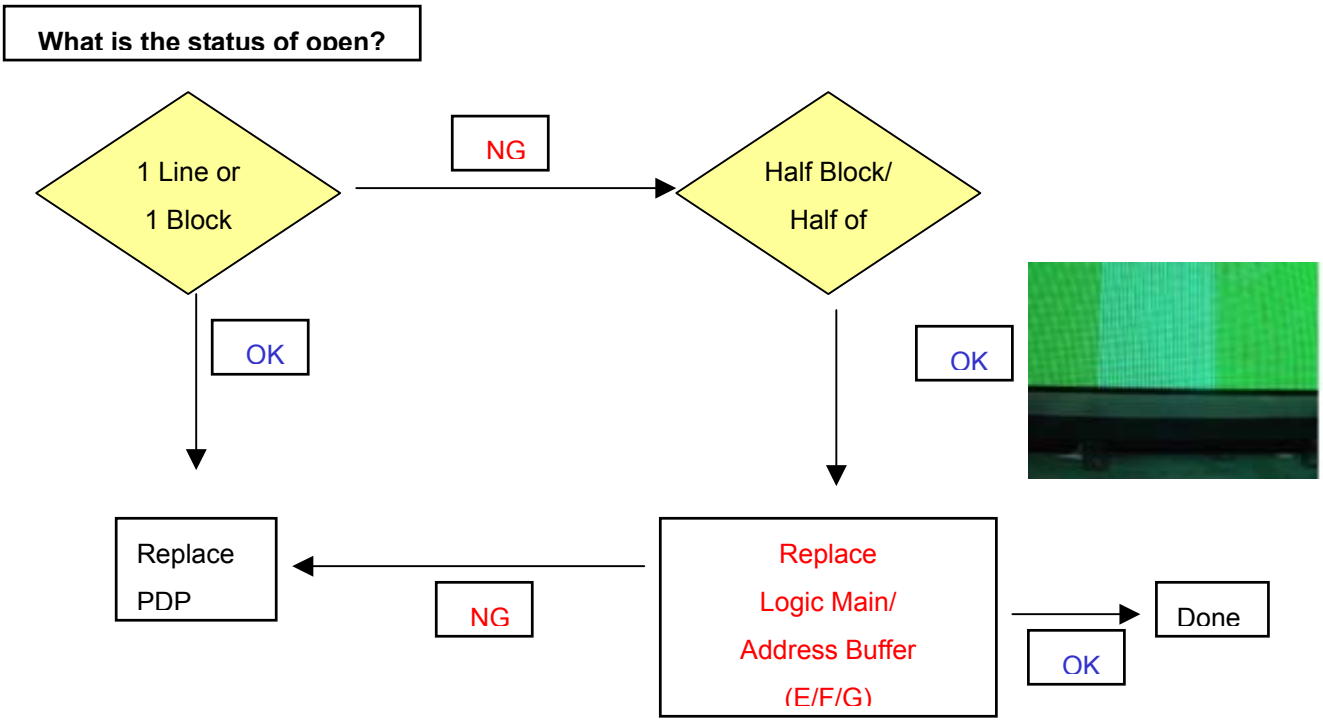
⇒ Address Open is related with Logic Main, Logic Buffer, FFC, TCP and so on.
This page shows you how to check the boards, and the following pages show you how to find the defective board.



4-1-7 Address Short (some vertical lines appear to be linked on screen

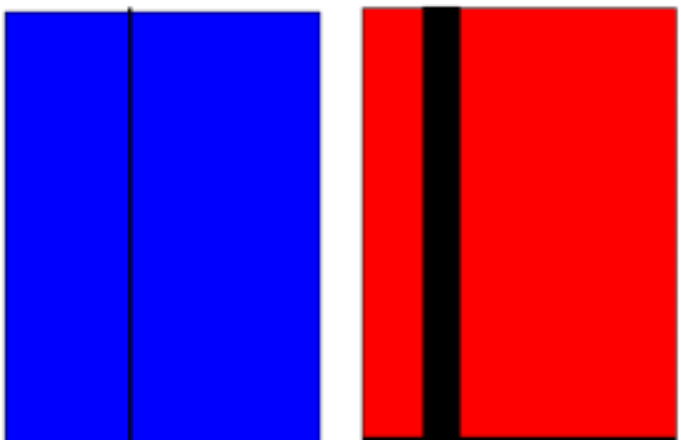
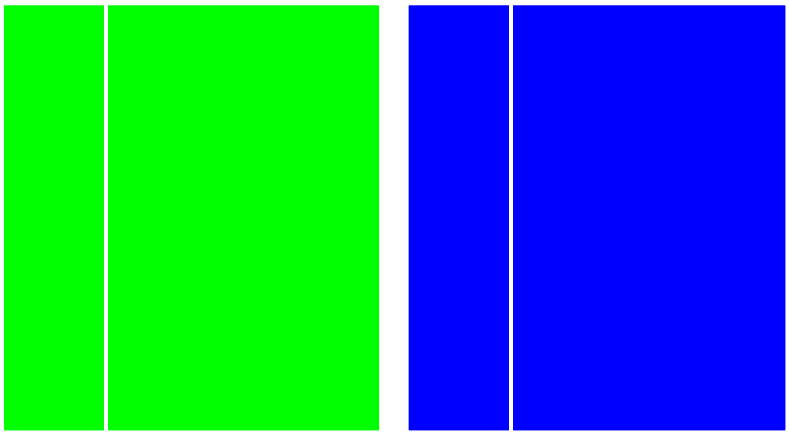
⇒ Address Short is related with Logic Main, Logic Buffer, FFC, TCP and so on.
This page shows you how to check the boards, and the following pages show you how to find the defective board.

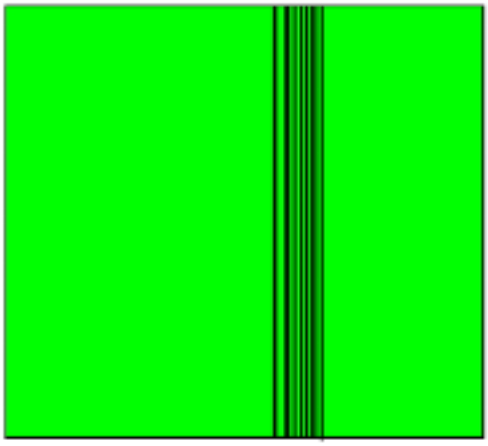
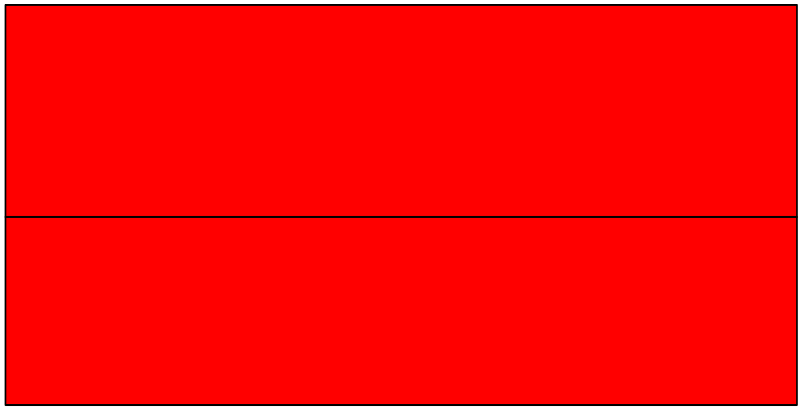


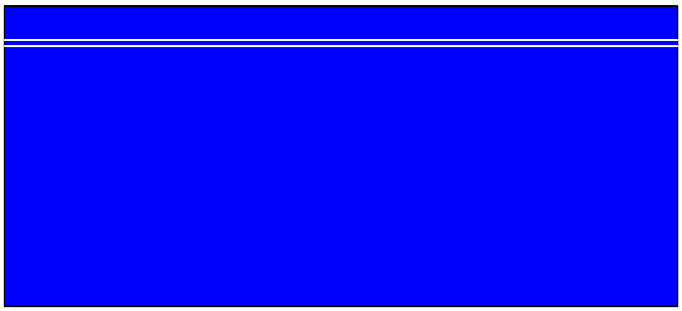
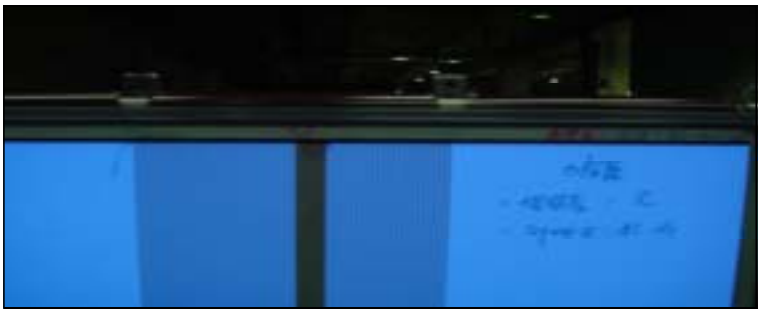


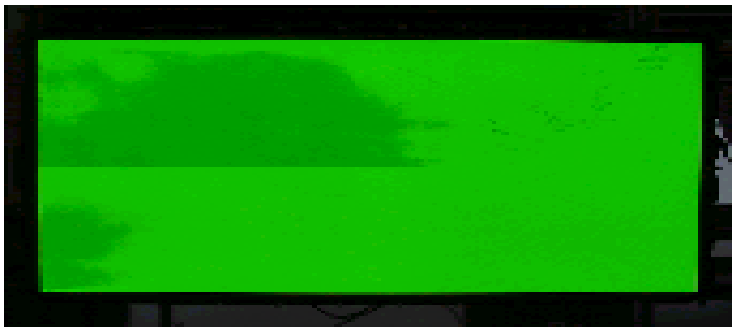
4-2 DEFECTS, SYMPTONS AND DETECTIVE PARTS

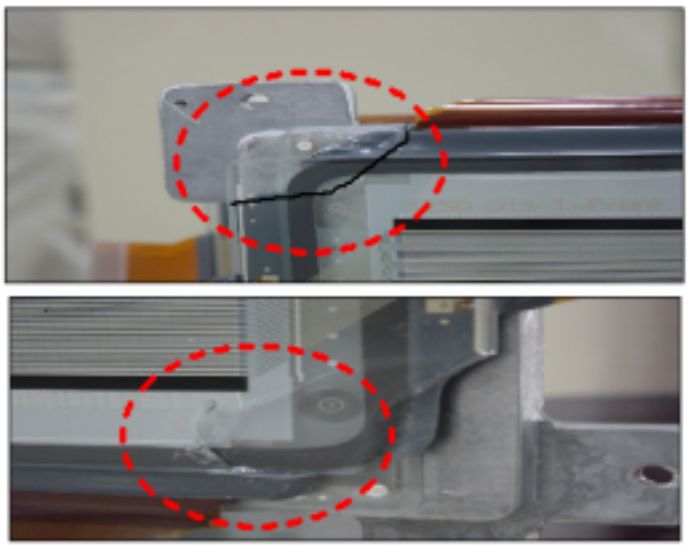
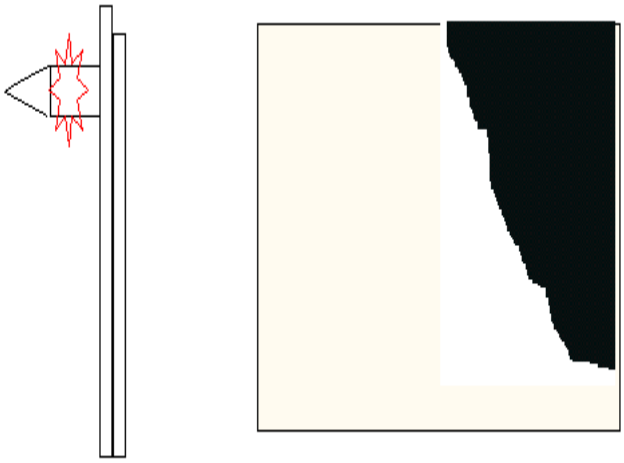
Condition Name	Description	Related Board
■ No Voltage Output	Operating Voltages don't exist.	PSU
■ No Display	Operating Voltages exist, but an Image doesn't exist on screen	Y-MAIN, X-MAIN, Logic Main, Cables
■ Abnormal Display	Abnormal Image(not open or short) is on screen.	Y-MAIN, X-MAIN, Logic Main
■ Sustain Open	some horizontal lines don't exist on screen	Scan Buffer, FPC of X / Y
■ Sustain Short	some horizontal lines appear to be linked on screen	Scan Buffer, FPC of X / Y
■ Address Open	some vertical lines don't exist on screen	Logic Main, Logic Buffer, FFC,TCP
■ Address Short	some vertical lines appear to be linked on screen	Logic Main, Logic Buffer ,FFC,TCP

Defect: Address(vertical stripe) Open	Defect: Address(vertical stripe) Short
■ Symptom : A line or block does not light up in address electrode direction.(1 line ,block open)  ■Cause ① manufacturing : Panel electrode single line/ foreign material./electrostatic/ TCP defect ② Parts : TCP, Board connection defect ③ Operation : Assembly error / Film damage	■ Symptom: Another color simultaneously appears because adjacent data recognizes the single pattern signal  ■Cause ① manufacturing : Panel electrode short / Foreign material conductive foreign object inside TCP ② Part : TCP/buffer defect lighting electrode cutting defect

Defect: Address output error	Defect: Sustain(horizontal stripe) Open
■ Symptom.: A defect other than address open and short Data printout signal error occurring at certain Gradation or pattern  	■ Symptom : One or more line do not light up in Sustain direction  ■Cause : ① manufacturing : .Panel bus electrode single line FPC pressure defect ② Parts : FPC/board/connection disconnection ③ operation : assembly error.

Defect: Sustain(horizontal stripe) Short	Defect: Dielectric material layer damage
■Symptom : Combined or adjacent lines are short in sustain direction. The line appear brighter than other at Ramp gradation pattern or low gradation patter  ■Cause ① manufacturing : Panel electrode short/Foreign material. ② Parts : Board/ connector/pin error ③ Operation : connector / assembling error	■ Symptom: Burn caused by the damage of address bus dielectric layer appears in the panel discharge/non discharge area. sustain also open/short occurs by the damage of address sustain printout  <Add Block and Line Open> <Add and Sustain Open> ■Cause : layer uneven / abnormal voltage / foreign material repair failed

Defext: F/White low discharge	Defect: Weak discharge
■Symptom : Low discharge caused by unstable cells occurring at full white pattern if high (60 degree) or normal temparature.	■Symptom : Normal discharge but cells appear darker due to weak light emission occurring mainly at low (5 degree) Full white/Red/Green/Blue pattern or gradation pattern
	
■ Cause ① Panel : MgO source / dielectric thickness cell pitch/phosphor ② Circuit : drive waveform/ voltage condition	■ Cause ① Panel : MgO deposition count and thinckness / aging condition ② Circuit : drive waveform/ voltage condition

Defect : panel damage	Defect: Exhaust pipe damage
■ Symptom : Panel crack or break. No image appears in some cause depending on the damaged parts and damage level.  ■ Cause ① Manufacturing : Flatness/palette pin interruption ② Operation : overload of panel corner / careless handling ③ Panel : Flatness / assembly error	■ Symptom. : Crack in break if exhaust pipe an image is partially lacking or the panel noise occurs depending on the damaged parts and with the passage of time  ■ Cause : Careless panel handling

5. Disassembling / Assembling

5-1 Tools and measurement equipment

5-1-1. Tools

1) (+) type Screw Drivers : to screw the screws
2) Air Blower
3) Earth Ring
4) Small Driver : to adjust potentiometer
5) Dummy Discharge Resistor : 2.4kOhm/10W

5-1-2. Measuring Equipment

1) Oscilloscope : 500MHz sampling
2) Probe : 10:1
3) Digital Multi-meter
4) Signal Generator

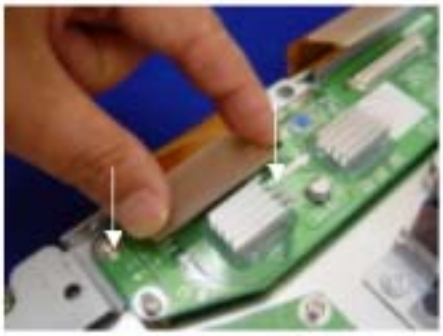
5-3 Disassembling & Re-assembling

5-3-1 Disassembling & Re-assembling of FPC (Flexible Printed Circuit) and Y-Buffer(Upper and Lower)

1. Removal procedures

1) Full out the FPC from Connector by holding the lead of the FPC with hands.

2. Assembling Procedures

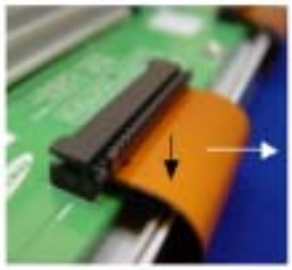


1) Push the lead of FPC with same strength until to be connected completely.

* Notice : Be careful do not get a damage on the connector pin during connecting by mistake.

5-3-2 Assembling & Disassembling of Flat Cable Connector of X-Main Board

1. Disassembling Procedure

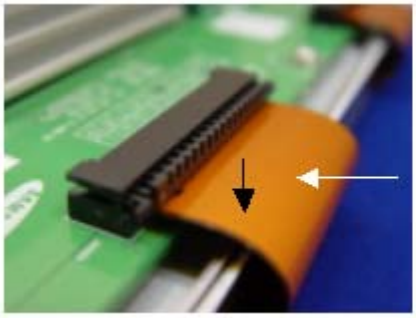


1) Pull out the clamp of connector.

2) Pull Flat cable out press down lightly.

3) Turn the Flat cable reversely.

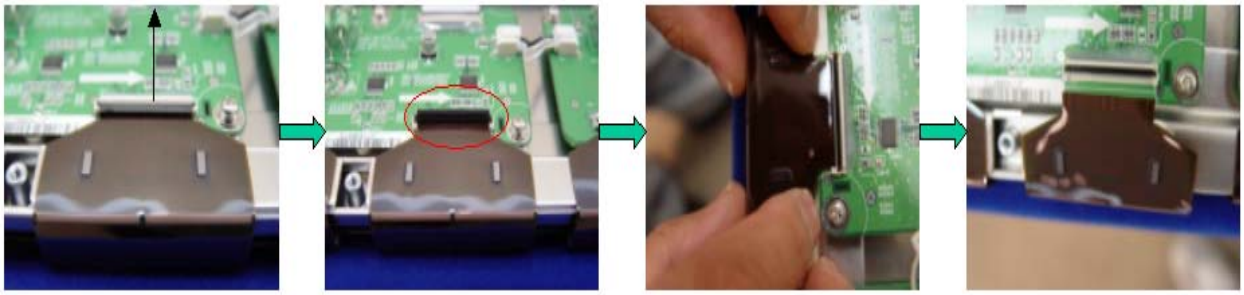
2. Assembling Procedure



1) Put the Flat cable into the connector press down lightly until locking sound (“Dack”) comes out.

5-3-3 Assembling & Disassembling the FFC and TCP from Connector

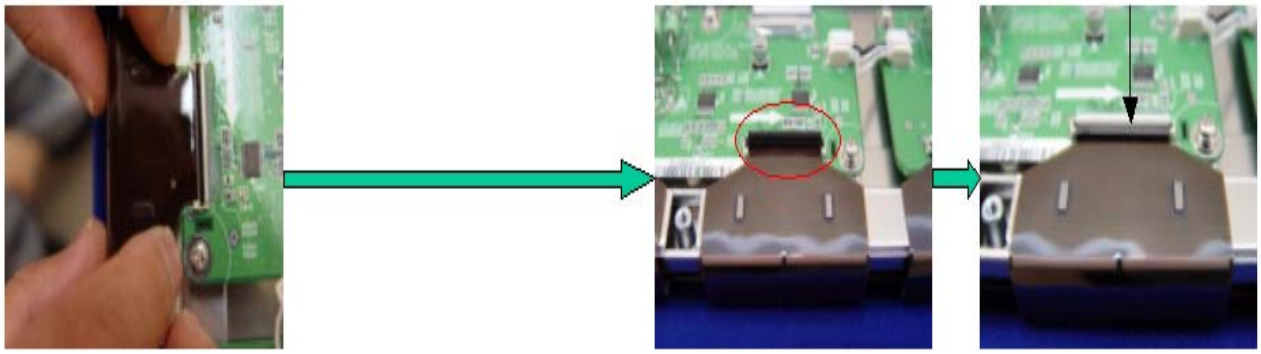
1. Disassembling of TCP



1) Open the clamp carefully.

2) Pull the TCP out from Connector.

2. Assembling of TCP



1) Put the TCP into the Connector carefully

2) Close the clamp completely.

(The sound (“ Dack”) comes out.)

* Notice : TCP and Connector was connected surely.

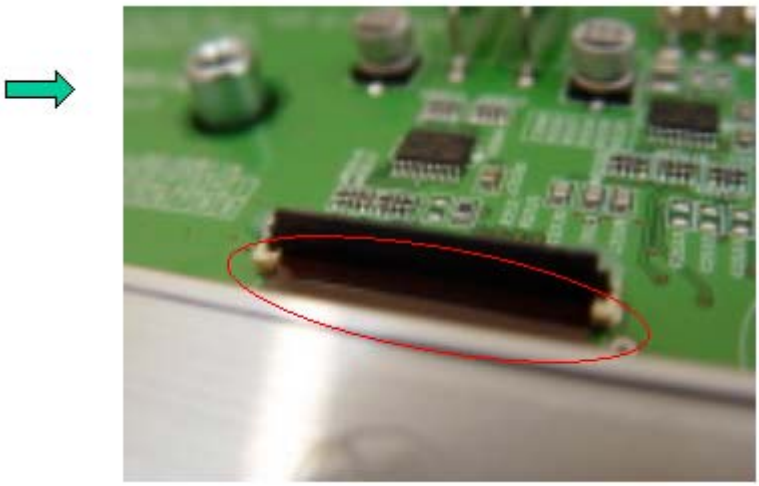
* Notice :

1) Checking whether the foreign material is on the Connector inside before assembling of TCP.

2) Be careful do not get a damage on the board by ESD during handling of TCP.

3. Misassembling of TCP

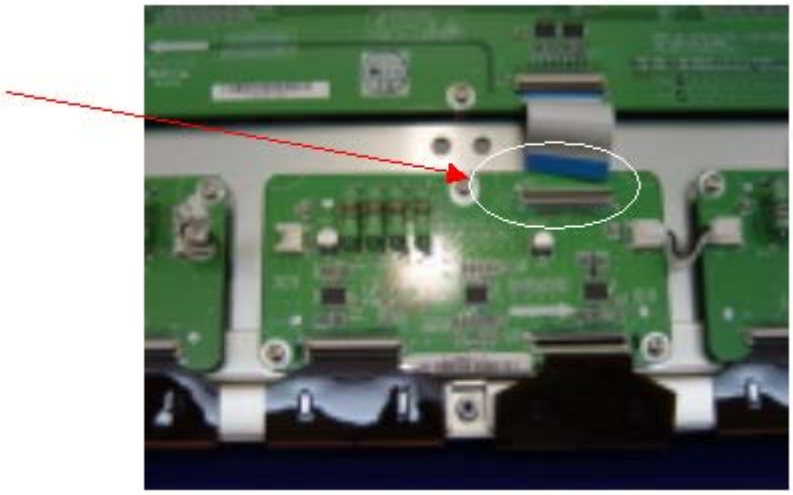
1) The misassembling of TCP is the cause of defect.



4. Checking method of misassembling of TCP

1)

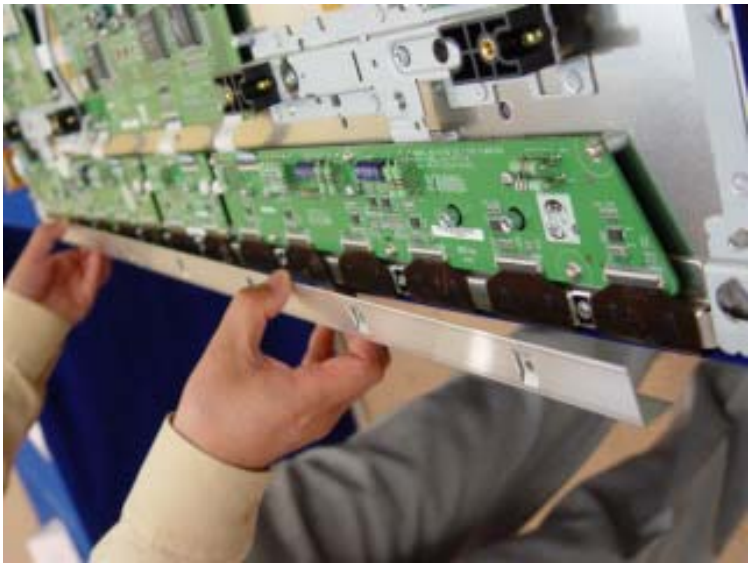
5. Assembling & Disassembling of FFC



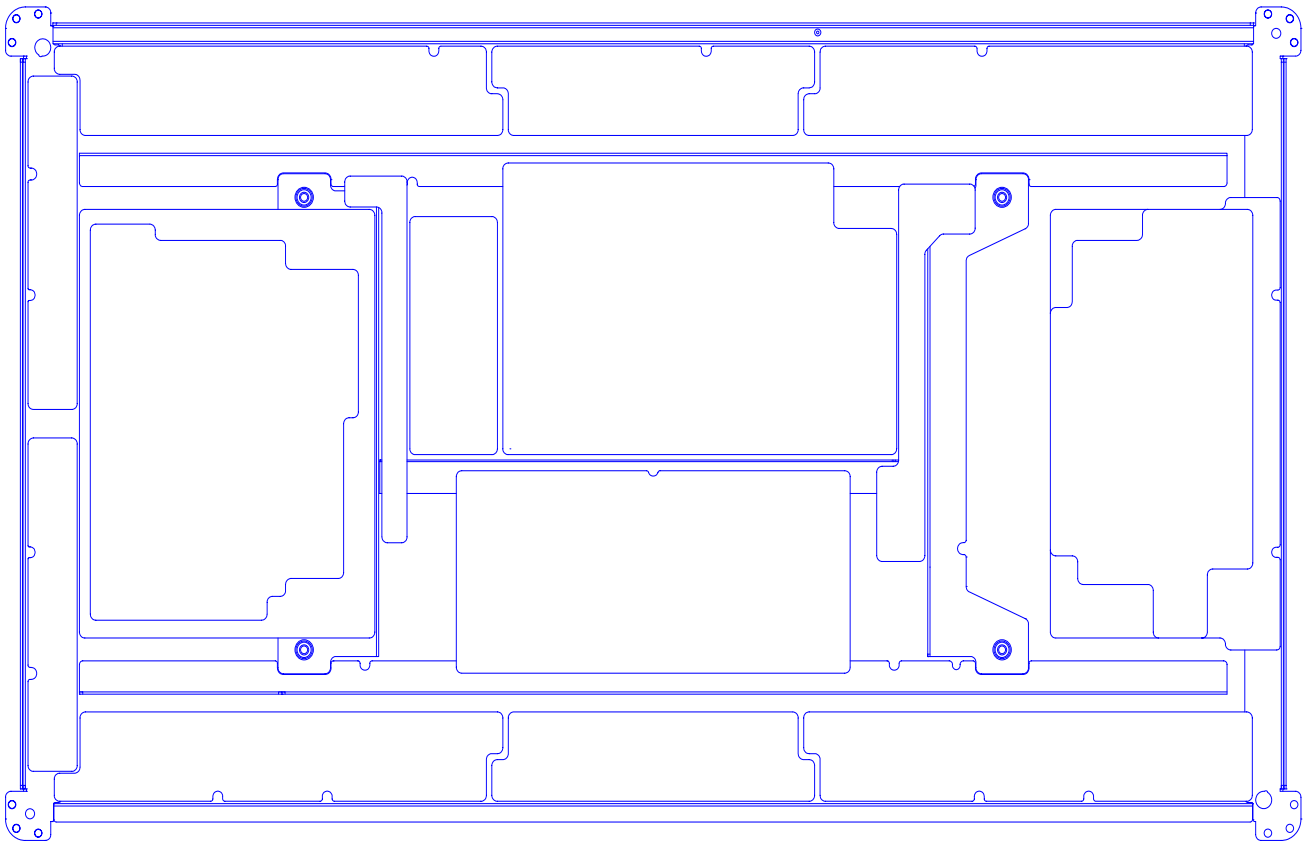
(This is the photo of the assembling of FFC)

The procedure of assembling and disassembling of FFC is the same as TCP.

5-3-4 Exchange of LBE, LBF, LBG board



(Photo 1)



(Photo 2)

1) Remove the screws in order of Center – Left Side – Right Side from heat sink and then get rid of heat sink. (Photo 1)
2) Remove the TPC, FFC and power cable from the connectors.
3) Remove all of the screws from defected board.
4) Remove the defected board.
5) Replace the new board and then screw tightly.
6) Get rid of the foreign material from the connector.
7) Connect the TCP,FFC and power cable to the connector.
8) Reassemble the TCP heat sink.
9) Screw in order of Right Side - Left Side - Center (Photo 2)

If you screw too tightly, it is possible to get damage on the Driver IC of TCP.

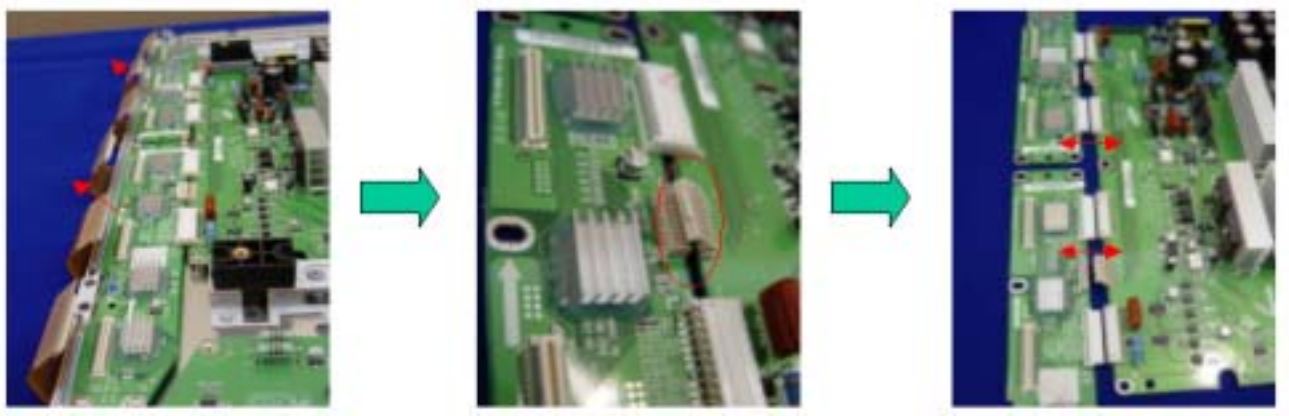
5-3-5 Exchange YBU, YBL and YM board

1) Separate all of the FPC connector of YBU (Y-Buffer upper) and YBL (Lower). (Photo 1)
2) Separate all of the connector of CN5001 and CN5008 from Y-Main.
3) Loosen all of the screws of YBU, YBL and YM.
4) Remove the board from chassis.

5) Remove the connector of CN5006 and CN5007 among YBU, YBL and YM.

6) Remove the YBL and YBU from Y-main.

7) Replace the defected board.



8) Reassemble the YBU and YBL to the Y-Main.

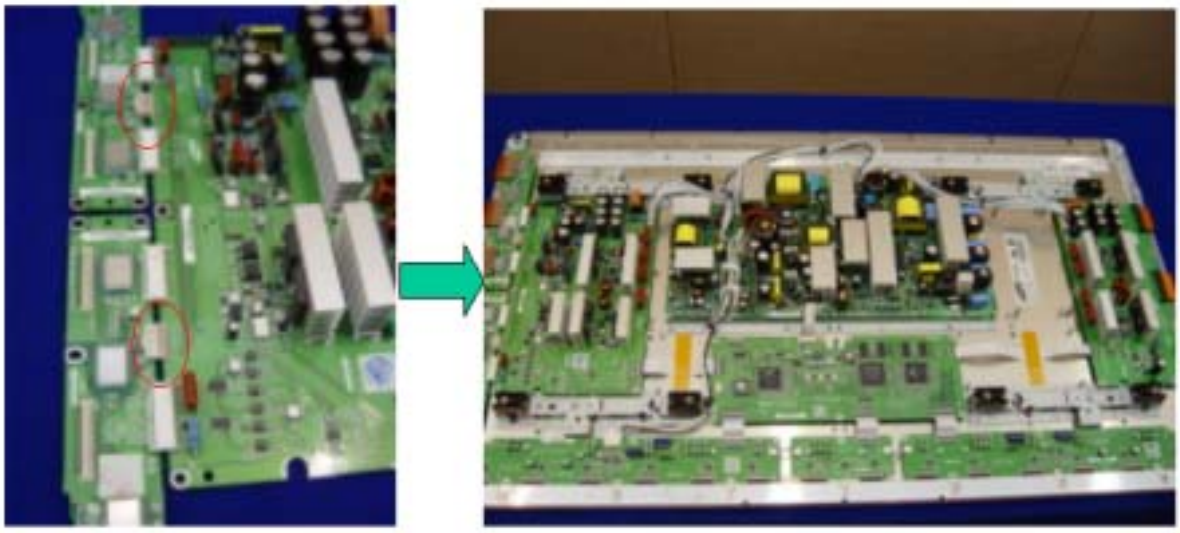
9) Connect the connector of CN5006 and CN5007 among YBU, YBL and YM.

10) Arrange the board on the chassis and then screw to fix.

11) Connect the FPC and YM of panel to the connector.

12) Supply the electric power to the module and then check the waveform of board.

13) Turn off the power after the waveform is adjusted.



6. Operation Check after Repair Service

6-1 Check Item

	Check Item	Specification	Remarks
Module assemble check	TCP Assembling condition	Securely connected or tightened	
	Drive board		
	Y BUFFER		
	Logic & Logic Buffer		
	Harness	Securely connected	
	Material Mixing	No material mixing	

6-2 Check Procedure

1) Visual check as following

a. Assembling condition of module.

b. No problem on the connection of module.

c. The grounding and easily short-circuited parts are not damaged.

2) Check the Dip Switch is setting [SW2000]

3) Turn on the power to PDP module, and then check that LED lights up and the SET is working well.

4) Check the power voltage after turn on the power, and then check the Display condition by tapping slightly the Y-FPC 2 or 3 times.

5) Check whether something wrong during Full White Pattern period.

6) If something wrong, each voltage should be set to the standard voltage by using Multi-Tester and adjusting tools.

7) Adjust the waveform, using Oscilloscope for the waveform adjusting point.

8) Check the discharge of front panel by changing the image for each pattern.

9) Check the Low-discharge, Over-discharge and panel condition by adjusting the Pattern Generator Level.

10) Discharge still remain send back to SDI

PD50HAASUSXS1-A01 AKAI R&D USA PDP5025M

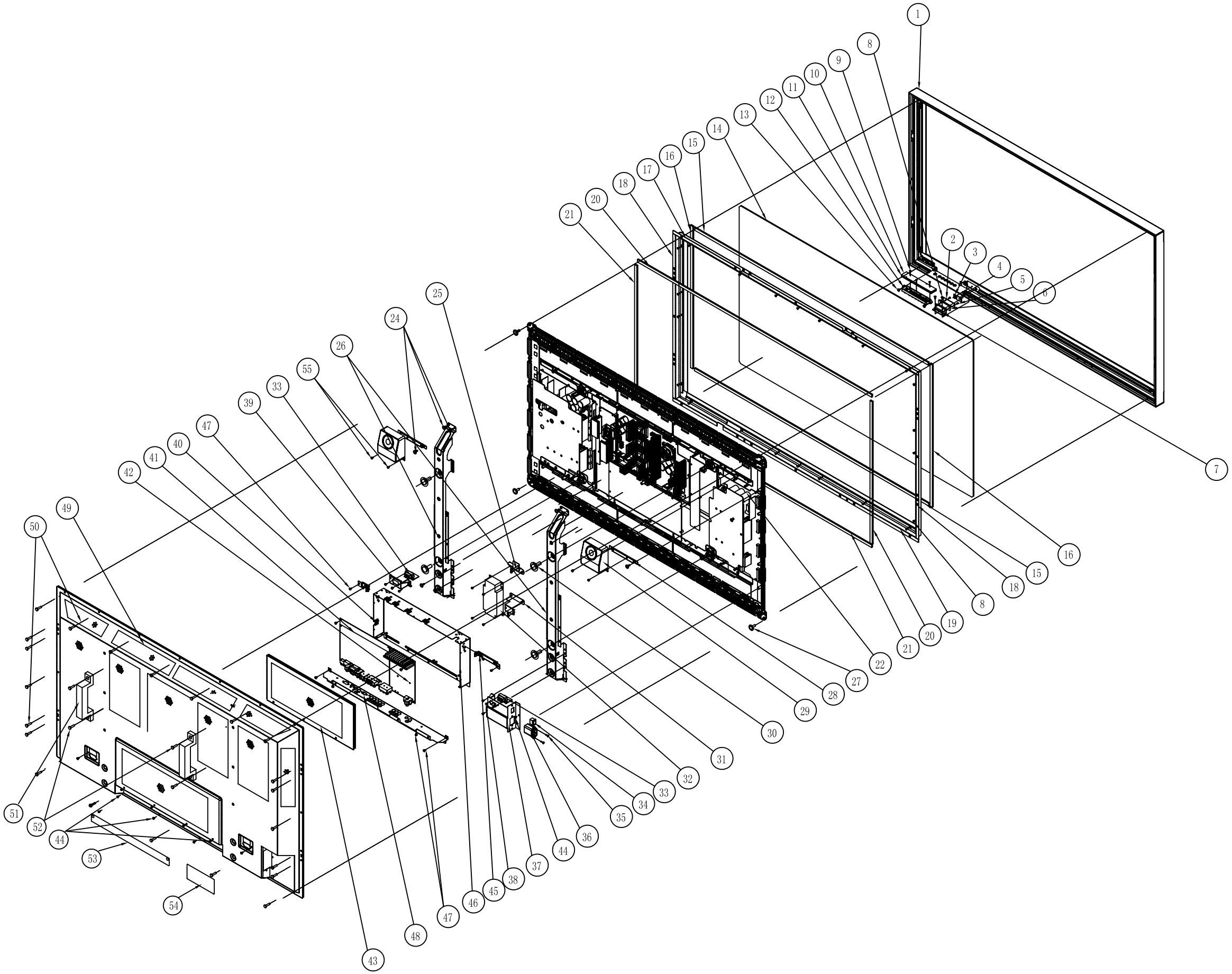
Item	Component	Description/Country Origin	Unit	Quantity
一, ELECT PART				
1	771-50AA03-01	KEY PCB ASSY	SET	1
2	771-50AA04-01	IR PECEIVE PCB ASSY	SET	1
3	771-50AA05-01	SPK JACK PCB ASSY	SET	1
4	771E50AA02-01	MAIN PCB ASSY	SET	1
5	771L50AA01-01	AUDIO PCB ASSY	SET	1
6	774M50AA02-01	MECH CHASSIS ASSY	SET	1
7	774P50AA02-01	POWER ASSY	SET	1
8	786-SPA103-02	INT. SPK ASSY	SET	1
9	E3403-004001	TUBE SUMITUBE D5.0 BLK 600V	M	0.1
10	E3421-926067	WIRE ASSY 1H2.5-2H2.5 L=200MM 31P (L	PCS	1
11	E3421-926068	WIRE ASSY 2.5 9P/11P L=190MM EMI	PCS	1
12	E3421-926069	WIRE ASSY 2.5 8P/10P+4P L=280MM EMI	PCS	1
13	E6205-002003	DISPLAY PDP 50" SDI-V3.0 (XGA) (127	PCS	1
14	E7801-08001	PCB ASSY POWER 240	SET	1
二, MECH PART				
1	244-34B811-01	GIFT BOX HANDLE 34B8	PCS	2
2	248-46D201-01	HANDLE FOR PLASMA	PCS	2
3	263-42D101-01S	POWER LENS 42D1	PCS	1
4	269-42D101-01L	REMOTE LENS 42D1	PCS	1
5	322-42P101-01	REMOTE LENS RUBBER SPACER PDP-42TP1	PCS	1
6	322-42P102-01	POWER LENS RUBBER SPACER PDP-42TP1	PCS	1
7	322-42P103-01	SEPARATE RUBBER SPACER FOR REMOTE AN	PCS	1
8	329-064510-50	SPONGE 645X10X5.0MM W/ADHESIVE	PCS	2
9	329-115010-50	SPONGE 1150X10X5.0MM W/ADHESIVE	PCS	2
10	361-101261-01	CABLE TIE	PCS	10
11	379-42P101-01	FILTER RUBBER BAG A PDP-42TP1	PCS	6
12	379-42P103-01	FILTER RUBBER BAR C 5.5X50X3.0MM W/	PCS	6
13	384-42D103-08H	PVC SHEET FOR AKAI PCB PD42HAA USA	PCS	1
14	387-50AA01-03H	MODEL PLATE AKAI ENG PDP5025M H	PCS	1
15	388-42D103-01H	CAUTION PLATE ENG 42D1 H	PCS	1
16	388-42P101-01	PC SHEET FOR REMOTE PCB 42P1 94V0	PCS	1
17	388-42SB04-01H	POWER PLATE SANSUI 42SB	PCS	1
18	388-50AA01-01H	SPEAKER L PLATE ENG (-/+)	PCS	1
19	388-50AA01-02H	SPEAKER R PLATE ENG (-/+)	PCS	1
20	400-50AA02-01	FRONT CABINET FOR SAMSUNG PANEL BLAC	PCS	1
21	402-50AA02-01S	BACK COVER FOR 50AD HARSPER	PCS	1
22	420-50AA01-01S	MAIN BRACKET	PCS	2
23	423-50AA01-01S	GLASS FILTER SUPPORT TOP	PCS	1
24	423-50AA02-01S	GLASS FILTER SUPPORT BOTTOM	PCS	1
25	423-50AA03-01S	GLASS FILTER SUPPORT L/R	PCS	2
26	424-50AA01-01S	POWER PCB BRACKET (A)	PCS	1
27	424-50AA02-01S	POWER PCB BRACKET(B)	PCS	1
28	429-50AA0C-01S	TERMINAL SPEAKER BRACKET	PCS	2

29	429-50AD07-01	REMOTE PCB BRACKET	PCS	1
30	429-50AD0C-01S	POWER JACK BKT	PCS	1
31	429-50AD0D-01S	SPEAKER JACK BRACKET	PCS	1
32	457-42D101-01	CLAMP ID=4.3MM L=46MM	PCS	3
33	486-50AD01-01	NAME PLATE AKAI SIL/BLACK 50AD	PCS	1
34	553-002509-40A	EMI SHIELD GASKET 25X9X4.0MM W/CONDU	PCS	4
35	553-005009-25A	SHIELD GASKET 50X9X2.5MM W/CONDUCTIV	PCS	2
36	553-006509-40A	SHIELD GASKET 65X9X4.0MM W/CONDUCTIV	PCS	4
37	553-015009-40A	EMI SHIELD GASKET 150X9X4.0MM W/COND	PCS	10
38	553-017009-40A	EMI SHIELD GASKET 170X9X4.0MM W/COND	PCS	2
39	553-018509-40A	EMI SHIELD GASKET 185X9X4.0MM W/COND	PCS	5
40	553-020009-40A	SHIELD GASKET 200X9X4.0MM W/CONDUCTI	PCS	2
41	553-067009-40A	EMI SHIELD GASKET 670X9X4.0MM W/COND	PCS	2
42	553-114009-40A	EMI SHIELD GASKET 1140X9X4.0MM W/CON	PCS	2
43	554-090030-01	SHIELD CLOTH 90X30MM W/CONDUCTIVE AD	PCS	1
44	563-119-	SERIAL NO. LABEL	PCS	1
45	568-P46T02-02	WARNING LB ENG 42SF NIL	PCS	1
46	579-42D103-02	ON/OFF LB ENG 42D1 NIL	PCS	1
47	579-42D105-01	PROTECTIVE EARTH LABEL FOR ESA 42TD1	PCS	1
48	579-50AA01-03	BAR CODE LABEL AKAI W/SERIAL NO PDP5	PCS	2
49	579-50AA02-01	DANGER CAUTION LABEL	PCS	1
50	579-50AD02-01	SERIAL NO/BAR CODE LABEL 50HA (USA)	PCS	1
51	580-P50AAHS-MU01	L IB E FOR AKAI PD50HAA MONITOR SDI SA	PCS	1
52	590-50AA01-02	WARRANTY CARD ENG AKAI PDP5025M	PCS	1
53	593-42D101-01	INSERTION CARD AKAI PDP4216M MONITOR	PCS	1
54	599-BM0502-02	IB SHEET E OF TEARDOWN FOR BM05 (50A	PCS	1
55	601-305008-00	MACH.SCREW CTS 3X8 BZN +	PCS	2
56	602-305004-10	MACH. SCREW PAN-WASHER M3X4 NIP +H	PCS	7
57	602-305006-00	MACH. SCREW PAN-WASHER 3X6 B ZNP +H	PCS	14
58	602-305006-10	MACH.SCREW WHR 3X6 NIP +	PCS	19
59	604-601020-00	MACHINE SCREW BINDING M6X1.0PX20MM B	PCS	6
60	60D-407010-40	MACH. SCREW W/SPRING WASHER M4.0X0.7	PCS	8
61	60D-508012-40	MACH. SCREW W/SPRING WASHER M5.0X0.8	PCS	4
62	60D-801235-00	MACHINE SCREW W/SPRING WASHER M8.0X1	PCS	4
63	610-300210-00	S-TAP.SCREW RND 3X10 A BZN +	PCS	4
64	623-401812-00	TAPING SCREW B-TYPE TRUSS 4X12 B ZNP	PCS	27
65	624-302406-10	TAP SCREW B-TYPE BINDING 3.0X6 WNC +	PCS	22
66	734-BM0501-02	STAND BM05	PCS	1
67	790-002517-A1	REMOTE CONTROL 0025	PCS	1
68	844-50AA01-01	WOODEN PALLET 1418X1115X116	PCS	0.333
69	900-500101-01B	DISPLAY FILTER 50" OPTIMAX (1155X67	PCS	1
三, PACKING				
1	300-50AA01-02C	POLYFOAM TOP 50HAA	PCS	1
2	300-50AA02-02C	POLYFOAM BOTTOM 50HAA	PCS	1
3	300-50AA03-01C	POLYFOAM BM05 STAND BASE PDP50	PCS	1
4	310-111404-07V	POLYBAG 11"X14"X0.04	PCS	1
5	310-633810-02T	POLYBAG 63"X38"X1.0MM W/WARNING &REC	PCS	1

6	510-50AA03-01K	GIFT BOX 1418X902X370 PDP5025 AKAI (	PCS	1
7	512-50AA01-01	SHEET 1418X1316	PCS	0.333
8	518-50P111-01K	BOTTOM BOX 50HAB/50HSB	PCS	1
9	E3404-157004	AC CORD UL 1.88M (YY-3/ST3 YUNBIAO)	PCS	1
10	E7301-011002	BATTERY AA R6P1.5V <2>	PCS	2

NOTE : THIS RELEASED DRAWING WAS PRODUCED BY COMPUTER, DO NOT UPDATE MASTER MANUALLY

DWG.Rev.	ZONE	DESCRIPTION	DATE	REVISOR



ITEM	PART NO.	DESCRIPTION	QTY	REMARK
55	602-305008-10	PAN-WASHER 3X8 B ZNP =H	4	
54	387-50AA01-03H	MODEL PLATE AKAI ENG PDP5025M	1	
53	384-42D103-08H	PVC SHEET FOR AKAI PCB PD42H	1	
52	604-601020-00	MACH. SCREW M6X20	4	
51	248-P46U02-01	HANDLE	2	
50	623-401812-00	TAPING SCREW B-TYPE TRUSS 4X12 B ZNP +H	27	
49	402-50AA02-01S	BACK COVER	1	
48	436-50AA07-01S	TERMINAL SHEET	1	
47	602-305004-10	MACH. SCREW PAN-WASHER M3X4	21	
46	481-50AA03-01S	SHIELD BOX BOTTOM	1	
45	429-50AA0B-01S	BKT B FOR SHIELD BOX 50AA	1	
44	602-305006-00	PAN-WASHER 3X6 B ZNP =H	14	
43	483-50AA01-01	SHIELD BOX COVER	1	
42	771L50AA01-01	AUDIO PCB ASSY FOR PD50HAA SANSUI PW181 CHASSIS USA	1	
41	771E50AA02-01	MAIN PCB ASSY FOR PD50HAA SANSUI PW181	1	
40	367-42D101-01	EDGE SADDLE 14MM	5	
39	429-50AD0D-01S	SPEAKER JACK BRACKET	1	
38	614-300108-00	S-TAP. SCREW BINDING 3X8 BIG+	4	
37	429-50AD0C-01S	POWER BKT	1	
36	E4405-035001	AC LINE FILTER	1	
35	601-305008-10	MACH. SCREW 3X8	2	
34	E4101-027001	POWER SWITCH	1	
33	E3701-051020	PCB ASSY SPEAKER OUT BOARD 30X	2	
32	E7801-080001	PCB ASSY POWER 24V FOR SDI-V4	1	
31	424-50AA02-01S	POWER PCB BRACKER (B)	1	
30	60D-801235-00	MACHINE SCREW W/SPRING WASHER M8X35	4	
29	E4801-116002	SPEAKER 16 OHM 7W D2"	2	
28	429-50AD0C-01S	TERMINAL SPEAKER BRACKET	2	
27	60D-508012-40	W/SPRING WASHER M5.0X0.8X12MM WHITE ZIN/P	4	
26	420-50AA01-01S	MAIN BRACKET	2	
25	424-50AA01-01S	POWER PCB BRACKER (A)	1	
24	60D-407010-10	MACH. SCREW W/SP WASHER 4X10	8	
23	457-42D101-01	CLAMP	5	
22	E6205-002003	DISPLAY PDP SDI-WXGA 50"	1	
21	326-064510-50	SPONGE CUSHION 645X10X5.0MM W/ADHESIVE	2	
20	326-115010-50	SPONGE CUSHION 1150X10X5.0MM W/ADHESIVE	2	
19	423-50SB07-01S	FILTER SUPPORT BTM	1	
18	423-50SB03-01S	FILTER SUPPORT L&R	2	
17	423-50SB06-01S	FILTER SUPPORT TOP	1	
16	553-067009-40A	670X9X4.0MM W/CONDUCTIVE ADHESIVE	2	
15	553-114009-40A	1140X9X4.0MM W/CONDUCTIVE ADHESIVE	2	
14	900-50AA01-01	DISPLAY FILTER 50" OPTIMAX	1	
13	602-305006-10	MACH-SCREW WHR 3X6	29	
12	277-42D101-XXS	FUNCTION KNOB	1	
11	771-42D101-01	KEY PCB	1	
10	388-42D101-01	PC SHEET FOR KEY PCB	1	
9	614-260208-10	STP SCREW 2.6X8	3	
8	624-302406-10	TAP SCREW B-TYPE BINDING 3X6 WNC +H	22	
7	429-45AD07-01	REMOTE PCB BRACKET	1	
6	771-42D103-01	REMOTE PCB	1	
5	604-305005-30	MACH.SCREW BID 3X5	2	
4	269-42D101-01L	REMOTE LENS	1	
3	263-42D101-01S	POWER LEN	1	
2	388-42D102-01	PC SHEET FOR REMOTE PCB	1	
1	400-50AA02-01	FRONT CABINET	1	

DRAWN.					
CHECKED					
APPRD.					
3rd ANGLE PROJECTION					

TOLERANCE UNLESS OTHERWISE SPECIFIED

0 ~ 30	± 0.10
>30~100	± 0.20
>100	± 0.30
ANGULAR:	± 0.3°
UNIT :	mm

KAWA ELECTRONIC R & D CENTRE

MATL.

FINISH

TITLE EXPLODE DRAWING (5025M)

MODEL NO. 50HAA

A2 | PART NO. | DWG. NO.

SCALE NIL | SHEET 1 OF 1

If you forget your V-Chip Password

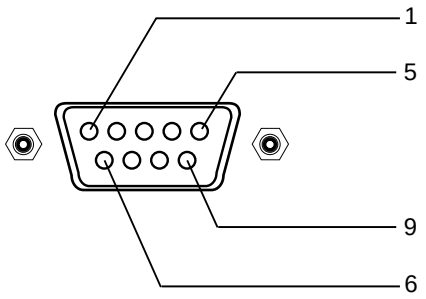
- Omnipotence V-Chip Password: **5898.**
- Press **MENU** button.
- Press **Up, Down** and CH+, CH-buttons to highlight "V-Chip" Control.
- Press OK button to pop up "INPUT PASSWORD".
- Use the Number buttons (0~9) to enter the omnipotence Password 1234.
- Press Down to highlight "Password change" Control.
- Press **OK** button to confirm and will pop up "Password Change" item.
- Change to your familiar Password again.

Software upgrade

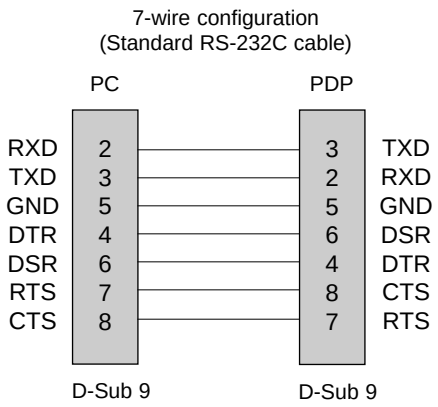
- Connect the RS-232C input jack to an external control device (such as a computer) and software upgrade.

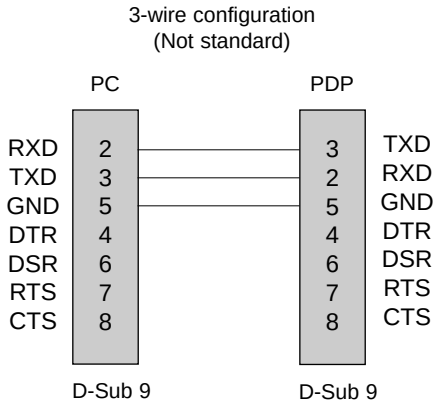
Type of connector; D-Sub 9-pin male

No.	Pin name
1	No connection
2	RXD (Receive data)
3	TXD (Transmit data)
4	DTR (DTE side ready)
5	GND
6	DSR (DCE side ready)
7	RTS (Ready to send)
8	CTS (Clear to send)
9	No Connection



RS-232C configurations





Software upgrade Process

- Power Switch OFF.
- Connect the serial port of the control device to the RS-232 jack on the PDP back panel.
  RS-232C connection cables are not supplied with the PDP.
- Power Switch ON. The power indicator on the front of the panel should now display red, means that the PDP is in standby mode.
- Copy the software (Flash Upgrader) to the computer.
- Open the software (Flash Upgrader.exe)
- Point "Flash" on the interface of the Flash Upgrader.exe.
- Press STANDBY button on the front panel or POWER button of Remote control, Power indicator green, the PDP is in power ON mode, software start upgrader immediately.
- Waiting for the upgrader programing, when it is finished, the PDP will auto power on.
- After the upgrader is finished, shut down the power switch, take out the RS-232C connection after the power indicator is extinguished.

Note: The computer and PDP must be keep **Power ON** in the software upgrade processing.